Mask Set Errata for Mask 1N52N

This report applies to mask 1N52N for these products:

- K32L2A41VLL1A
- K32L2A31VLL1A
- K32L2A41VLH1A
- K32L2A31VLH1A

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
ERR050117	FAC: Execute-only access control feature has been deprecated
ERR009464	FIRC: A transfer error is received when writing to the SCG_FIRCSTAT register
ERR009380	FlexIO: Reading FlexIO register when FlexIO functional clock is disabled results in a bus hang
ERR009364	LPI2C: HS-mode signal on Repeated START uses Fast mode timing for the (Repeated) START hold time
ERR009365	LPI2C: Master does not always end the transfer when the NACK detect flag is set

Table 2. Revision History

Revision	Changes
11Sep2019	Initial revision

ERR050117: FAC: Execute-only access control feature has been deprecated

Description: The FAC feature is no longer recommended for use.

Workaround: Do not program the XACCn registers to use the FAC feature.

ERR009464: FIRC: A transfer error is received when writing to the SCG_FIRCSTAT register

Description: When writing to the SCG_FIRCSTAT register, a transfer error occurs that causes the code execution to stall at the write point. The SCG_FIRCSTAT register is used to trim FIRC, which is already trimmed at the factory.

Workaround: Do not use the SCG_FIRCSTAT register to trim FIRC as it is already trimmed at the factory.

ERR009380: FlexIO: Reading FlexIO register when FlexIO functional clock is disabled results in a bus hang

Description: Accessing a FlexIO register when the FlexIO functional clock is disabled (the clock source configured to 0 in PCC_FLEXIO0[PCS], or the selected clock source is disabled) will hang the bus and the access will stall forever.

Workaround: Always enable the FlexIO functional clock before accessing any FlexIO register.

ERR009364: LPI2C: HS-mode signal on Repeated START uses Fast mode timing for the (Repeated) START hold time

Description: The internal HS-mode signal on Repeated START updates after the (Repeated) START hold time, which causes the (Repeated) START hold time to use the Fast mode timing in LPI2Cx_MCCR0 instead of the HS-mode timing in LPI2Cx_MCCR1. This action only affects the (Repeated) START hold time and only on a Repeated START, that initiates HS-mode. It does not affect the subsequent HS-mode data transfer. This issue occurs when the first START is at the normal speed and the second START is in the HS-mode.

Workaround: This issue only lengthens a hold time delay in HS mode and does not affect the HS mode protocol.

ERR009365: LPI2C: Master does not always end the transfer when the NACK detect flag is set

Description: When the NACK detect flag is set, the LPI2C master should terminate the existing transfer and block a new transfer until the flag clears. However, when the NACK detect flag is set, and a Repeated START is queued as the next operation, then the LPI2C Master does not terminate the transfer and instead continues the transfer until a STOP condition is sent. This satisfies the requirement of the I2C specification, but does not halt the transfer when it detects an unexpected NACK.

Workaround: Confirm that both the NACK detect flag (NDF) and the end packet flag (EPF) in the LPI2Cx_MSR register are set before clearing the NACK detect flag. When both flags are set, write a STOP condition generation command (0x3FF) to the Transmit Data register and then clear the flags.

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