56F8366

Preliminary Chip Errata

56F8366 Digital Signal Controller

This document reports errata information on chip revision A. Errata numbers are in the form n.m, where n is the number of the errata item and m identifies the document revision number.

Chip Revision A Errata Information:

The following errata items apply only to Revision A 56F8366 devices. These parts are marked with date codes of 0419 or greater (bottom line of marking).

Errata Number	Description	Impact and Workaround
1.0	The FlexCAN can shorten the CRC delimiter bit appearing on the CAN bus.	Impact: The CRC delimiter bit appearing on the CAN bus can be shortened by transmitting the ACK bit present in a data frame earlier than expected. This could cause the transmitting node to retransmit the data. Workaround: If problems occur in transferring data reliably, select CAN timing parameters to ensure that bit sampling happens 1 time quanta earlier in the bit period than would otherwise be selected.
2.0	The OCCS shutdown function is not as restrictive as desired.	Impact: This is one of several safety interlocks to prevent a coding error from shutting down the part accidentally. Workaround: The OCCS ISR should explicitly check for a loss of reference clock status bit set prior to shutting down the OCCS.
3.0	Unable to read COP counter register.	Impact: Unable to read COP counter register when the PLL is not on. Workaround: Read COP counter when PLL is in use.
4.0	Command conflict when setting CCIF in the Flash Module.	Impact: If CCIF is set at the same time the CBEIF bit is cleared, only the set will occur. This gives the impression that a command has completed when in fact it is active. This can only occur on the last cycle of a pipeline operation. Workaround: Use driver software to avoid this issue.

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Errata Number	Description	Impact and Workaround
5.0	Flash program/erase operations can cause other peripheral register access to be duplicated.	Impact: This condition can cause issues with the transmit/receive registers and quadrature decoder hold registers. Workaround: Avoid peripheral I/O to any peripheral except the Flash module for two (2) CPU cycles prior to writing to a Flash memory over its system bus interface.
6.2	The LVI interrupt signal polarity in STOP mode is inverted. *In Rev 2.0, clarified errata impact and workaround.*	Impact: The processor will not enter STOP mode if LVI is enabled or LVI IPL is set in the IPR2. Workaround: Disable LVI interrupt and clear LVI IPL. With this workaround, LVI will not wake up the processor from STOP mode.
7.0	The setting of the CHNCFG bits in the ADCR1 register for the mux channels associated with converter 0 override the settings for the mux channels associated with converter 1.	Impact: This problem affects scans with a mix of single-ended and differential mode conversions. If AN0/2-AN1/3 is set for single-ended conversions, then AN4/6-AN5/7 can't properly execute differential conversions. Similarly, if AN0/2-AN1/3 is set for differential conversions, then AN4/6-AN5/7 can't properly execute single-ended conversions. Settings for differential mode for converter 1 also adversely affect single-ended conversions in converter 0. Workaround: Restrict conversion types so that the cases described do not occur.
8.0	Wait mode operation is inconsistent in debug mode.	Impact: WAIT appears to work properly when the device is in mission mode. In debug mode, the WAIT instruction sometimes has no effect. Workaround: Test WAIT mode operation outside of the debug environment.
9.0	The EOnCE registers use the wrong clock. I/O fails in presence of holdoffs.	Impact: Real-time debugging not available. The EOnCE reads will fail in the presence of holdoffs. Workaround: For EOnCE writes, use NOP padding. No workaround is available for EOnCE reads in presence of holdoffs.
10.0	Software breakpoint in uninterruptable code can cause the debugger to execute instructions in the wrong order.	Impact: Same as description. For example, a conditional branch followed by two single word instructions with DBGHALT replaces the first instruction after the conditional branch. Workaround: CodeWarrior has implemented a workaround which uses NOP padding.

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Errata Number	Description	Impact and Workaround
11.0	The SCI TIDLE flag may not be cleared immediately upon transmission of a break character via the SBK bit of the SCI control register.	Impact: This can result in a premature transmitter IDLE interrupt. This only occurs when using the SBK bit of the SCICR to transmit break characters. Workaround: Poll the TIDLE bit of the SCI status register. Do not enable interrupts until TIDLE goes low. IF polling for TIDLE high, make sure that it is seen going low first before responding to TIDLE high. Make sure that TIDLE is cleared and then later set after transmitting break characters.
12.0	The interrupt controller uses the COP reset vector at startup if the COPR bit in the SIM_RSTSTS register is set, even if the current reset is not COP reset.	Impact: Same as description. Workaround: Clear the SIM_RSTSTS as part of the startup procedure.
13.0	The EOnCE OPDBR register will not work properly if there is more than one JTAG serially connected device used in a scan chain configuration.	Impact: This register is used for executing instructions shifted in by the host through the JTAG when the device is in debug mode. The intended instruction will not be executed under this condition. Note: This does not affect boundary-scan operation, which will still work properly no matter in what position the device is placed in the boundary-scan chain. Workarounds: 1. Each device must be on a separate scan chain for debugging purposes. 2. If there is only one 56800E device on a scan chain, then the EOnCE OPDRB register will work properly as long as the 56800E device is the first device on the scan chain.
14.0	The CodeWarrior debugger is not sensitive enough to the operation frequency of the device. Memory code may be corrupted when setting/ clearing.	Impact: Once the PLL is engaged, the device may be under erased/programmed when setting and clearing breakpoints. Workaround: The flash.cfg file should contain the following entry: `set_hfmclkd 0x14` This sets the on-chip Flash interface unit to use the maximum program time at 4 MHz system rate. At 60 MHz, program/erase times will be shorter than desired, but appear operational under otherwise normal conditions. Use of hardware breakpoints also eliminates this issue.

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Errata Number	Description	Impact and Workaround
15.0	With a Quad Timer counter, and when using a single compare register to generate timing intervals and clocking the timer at a rate other than at the IPbus_clock rate, the timer may count incorrectly when the compare register is changed.	Impact: When the compare register matches the counter register and is updated before the next timer clock the counter increments/decrements instead of reloading. Workarounds: 1. Use both compare registers, such that the inactive compare register is updated for use in the next count period. 2. Instead of updating the compare register, design the software so the LOAD register can be updated, with the compare register held constant. An in-depth discussion of this issue is presented in an FAQ available on the Freescale web page, www.freescale.com (perform a keyword search for “faq-25527”).
16.1	GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written.	Impact: Hardware designs that have asynchronous interruptable inputs on the same GPIO port cannot rely on the device to generate the interrupt. Workarounds: 1. Use different ports for these two interrupts. 2. After writing to the IESR, read the RAW_DATA register to determine if any other inputs have occurred at that instant.
17.2	With the Quad Timer, when Count Mode (CM) is 0b110 (edge of secondary source triggers primary count till compare) and the Output Mode (OM) is 0b111 (enable gated clock output while counter is active), the OFLAG will incorrectly output clock pulses prior to the secondary input edge if the primary count source is not an IPBus clock/N.	Impact: This will typically occur when an application is trying to output a finite number of 50% duty cycle clock pulses triggered by the output of another timer. Timer 1 creates an infinite pulse train which is fed into the primary input of Timer 2. Timer 2's secondary input is the triggering signal. Timer 2 must wait until the trigger and then count out the correct number of clock pulses. Workaround: The workaround is to rearrange functionality. Timer 1 uses an IPBus/N to generate a pulse train at 2x the desired clock rate. It uses CM = 0b110 and OM = 0b111 correctly. Then Timer 2 must convert the 2x pulse stream into a clock pulse stream at 1x frequency and 50% duty cycle. It does this by using CM = 0b001 (count rising edges of primary input) and OM = 0b011 (toggle OFLAG on successful compare) with a compare value of zero.

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Errata Number	Description	Impact and Workaround
18.4	Access to any field of a FlexCAN Message Buffer (MB) during reception or transmission of an extended ID frame's CRC and EOF may cause unwanted message reception.	Impact: With extended ID frames, if the ID_HIGH received matches the ID_HIGH configured in a receive MB, the frame will be received to this MB irrespective of the ID_LOW and the mask. So unwanted messages which should be filtered by the hardware mask register may be received. This issue only happens to the messages with the extended ID when ID_HIGH of the receive MB is equal to that of the current receiving frame. Messages with standard ID have no such issue. Workaround: Perform one of these actions, either a or b: a. Use only the Standard ID format for all messages, not the extended format. b. In case extended IDs are used, make sure that only ID bits 28 to 15 are used as the filter criteria, so that other ID bits (ID bits 14 to 0) are not used to filter messages. ID bits 14 to 0 may contain information not used for message filtering purposes.

19.5	If runtime flash programming is desired, Power-on reset (POR) of the device may not be fully effective for slow rise times of V_{DD} and/or V_{DDA}, on some small fraction of parts.	Impact:
		It may not be possible to write to the flash if the reset cause is not a software reset.
		
		Workaround:
		If runtime flash programming is desired, add the software reset in startup code if the reset cause is not a software reset. Example code:
		`If bit SWR of RSTSTS register is not set`
		`Set logical 1 to bit SWRST of SIM_CONTROL Register`
		`While loop (to wait for reset)`
		`else (continue with startup code)`

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The following errata items apply only to Revision A 56F8366 devices. These parts are marked with date codes of 0419 or greater (bottom line of marking).

Errata Number	Description	Impact and Workaround
20.6	FlexCAN transmit buffer activation at a node during a message's CRC and EOF reception at that node can either corrupt the received messages's ID_LOW at that node (see impact 1) or corrupt the message screening at that node (see impact 2).	Impact: 1.Expected message is received, but the ID_LOW field contains the wrong information. 2.Unwanted messages which should be filtered by the hardware mask register are received. The ID fields (ID_HIGH and ID_LOW) of the Receive Message Buffer are modified to this unwanted message ID. Workaround (for both 1 and 2): Activate transmit buffers when neither the CRC nor the EOF reception can be concurrent. Use the following procedure to activate transmt buffers: 1) Disable the Mailbox (MB) interrupt by using the FCMSGBUF bit in the interrupt priority register of the interrupt controller module. 2) Check the IDLE and TX/RX bits in the Error and Status Register (FCSTATUS). If IDLE bit = 1, or TX/RX bit =1, continue with step 3-7; otherwise jump to step 7. 3) Write the Control/Status word to hold the transmit MB inactive. 4) Write the ID_HIGH and ID_LOW. 5) Write the Data bytes. 6) Write the Control/Status word (active CODE, LENGTH). 7) Enable the MB interrupt.

Errata Sheet History

Previously Documented in Past Errata Sheets	Correction
GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written.	New item in Rev 1 of this errata sheet
With the Quad Timer, when using Count Mode (CM) 0b110 “edge of secondary source triggers primary count till compare” and the Output Mode (OM) is 0b111 “enable gated clock output while counter is active”, the OFLAG will incorrectly output clock pulses prior to the secondary input edge if the primary count source is not an IPBus clock/N.	New item in Rev 2 of this errata sheet
FlexCAN transmit buffer activation at a node during a message's CRC and EOF reception at that node can either corrupt the received messages's ID_LOW at that node or corrupt the message screening at that node.	New item in Rev 3 of this errata sheet.
Revise erratum 18.4.	Provide updated information on this erratum.

Errata Sheet History

Previously Documented in Past Errata Sheets	Correction
If runtime flash programming is desired, Power-on reset (POR) of the device may not be fully effective for slow rise times of V_{DD} and/or V_{DDA}, on some small fraction of parts.	New item in Rev 5 of this errata sheet.

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MC56F8366E
Rev. 6
07/2010