Mask Set Errata for Mask 1M25G

Introduction

This report applies to mask 1M25G for these products:

- MC9S08EL32
- MC9S08EL16
- MC9S08SL16
- MC9S08SL8

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0J27F. All standard devices are marked with a mask set number and a date code.

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "0301" indicates the first week of the year 2003.

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

SE193-CHSUM-OVERFLW: Checksum compare logic includes an overflow carry

Errata type: Silicon
Affects: SLIC
Description: The logic behind the checksum comparison performed by the receiving SLIC module wrongly executes an add with carry. The LIN protocol specifies an add without carry. This does not affect the SLIC's calculation of the checksum, but only the comparison of the transmitted message checksum value to the checksum calculated from the transmitted message data.

This has no effect when the correct checksum is transmitted, and it has no visible effect when an incorrect checksum is sent except in one singular case. When an incorrect checksum is sent, the SLIC still sees the error, as the sum is not 0xFF, and then correctly sets the SLIC interrupt flag even if the compare logic uses the add with carry. The exception is when the checksum should be 0x00, but is sent as 0xFF. In this case alone, the checksum comparison is seen as correct as the receiver adds 0xFF and 0xFF along with the carry, and the SLIC calculates 0xFF instead of 0x1FE.

Workaround: Do not transmit data sequences which create a checksum of 0x00. As long as there are non zero values in the data (and ID if using extended checksum as per LIN2.1) the checksum value 0f 0x00 is mathematically not possible.

SE157-ADC-INCORRECT-DATA: Boundary case may result in incorrect data being read in 10-bit modes

Errata type: Silicon
Affects: ADC
Description: In normal 10-bit operation of the ADC, the coherency mechanism will freeze the conversion data such that when the high byte of data is read, the low byte of data is frozen, ensuring that the high and low bytes represent result data from the same conversion.

In the errata case, there is a single-cycle (bus clock) window per conversion cycle when a high byte may be read on the same cycle that subsequent a conversion is completing. Although extremely rare due to the precise timing required, in this case, it is possible that the data transfer occurs, and the low byte read may be from the most recently completed conversion.

In systems where the ADC is running off the bus clock, and the data is read immediately upon completion of the conversion, the errata will not occur. Also, in single conversion mode, if the data is read prior to starting a new conversion, then the errata will not occur.

The errata does not impact 8-bit operation.

Introducing significant delay between the conversion completion and reading the data, while a following conversion is executing/pending, could increase the probability for the errata to occur. Nested interrupts, significant differences between the bus clock and the ADC clock , and not handling the result register reads consecutively, can increase the delay and therefore the probability of the errata occurring.

Workaround: Using the device in 8-bit mode will eliminate the possibility of the errata occurring.

Using the ADC in single conversion mode, and reading the data register prior to initiating a subsequent conversion will eliminate the possibility of the errata occurring.

Minimizing the delay between conversion complete and processing the data can minimize the risk of the errata occurring. Disabling interrupts on higher priority modules and avoiding nested interrupts can reduce possible contentions that may delay the time from completing a conversion and handling the data. Additionally, increasing the bus frequency when running the ADC off the asynchronous clock, may reduce the delay from conversion complete to handling of the data.

SE156-ADC-COCO: COCO bit may not get cleared when ADCSC1 is written to

Errata type: Silicon
Affects: ADC

Description: If an ADC conversion is near completion when the ADC Status and Control 1 Register (ADCSC1) is written to (i.e., to change channels), it is possible for the conversion to complete, setting the COCO bit, before the write instruction is fully executed. In this scenario, the write may not clear the COCO bit, and the data in the ADC Result register (ADCR) will be that of the recently completed conversion.

If interrupts are enabled, then the interrupt vector will be taken immediately following the write to the ADCSC1 register.

Workaround: It is recommended when writing to the ADCSC1 to change channels or stop continuous conversion, that you write to the register twice. The first time should be to turn the ADC off and disable interrupts, and the second should be to select the mode/channel and re-enable the interrupts.

SE143-ICS: ICS Internal Reference Can Remain Enabled in Stop3 Mode

Errata type: Silicon
Affects: ICS
Description: When transitioning from FEI or FBI modes to FEE or FBE modes, the internal reference clock may remain active in stop3 mode if the STOP instruction is executed soon after the IREFST bit in the ICSSC register clears. This can lead to elevated stop3 I_{DD}.

Workaround: To ensure the internal reference clock is disabled before entering stop3, wait three internal reference clock periods after the IREFST bit has cleared before entering stop3. On a device with a trimmed internal reference, one period will be between 25.6 µs and 32 µs, therefore waiting 100 µs is adequate for all trimmed devices.

Or

To ensure the internal reference clock is disabled before entering stop3, transition into FEE mode and wait until the LOCK status bit indicates the FLL has attained lock before entering stop3 or transitioning into FBE mode and entering stop3.

SE120-IIC: Incorrect Clocking in 10-Bit Addressing Mode

Errata type: Silicon
Affects: IIC
Description: This erratum is relevant only for applications using 10-bit addressing mode and does not affect 7-bit addressing mode operations.

When hexidecimal values E0,E1,E4,E5,E8,E9,EC,ED,F0,F2,F4, or F6 are used as data in master receive slave transmissions from the IIC module using 10-bit addresses, the IIC clock may produce an incorrect number of pulses. This will result in IIC communication errors.

Workaround: Avoid using the values listed in the erratum description as data in any master receive slave transmission from the IIC module while in 10-bit addressing mode.

SE196-SLIC: SLIC Interrupted Frame

Errata type: Silicon
Affects: SLIC

Description: The Local Interconnect Network (LIN) specification 2.0 and later requires that a slave task always detects a break/sync sequence. Under specific conditions, the SLIC module does not always detect a new frame if it interrupts a frame that is currently being received. Both the following conditions must be met for the SLIC so that it fails to detect the new frame:

- the second frame, sent at the same LIN frequency, has a BREAK length that is shorter than the BREAK length of the existing frame.
- the falling edge of the second BREAK occurs between the rising edge of the first BREAK and the rising edge of the start bit of the SYNC 55 bytes.

The figure below shows the point in time during which the new frame may not be detected, assuming both messages are operating at the same frequency.

Workaround: The LIN Master implementation needs to be designed to prevent an existing frame from being interrupted during the period indicated in the figure below, assuming both messages are operating at the same frequency.

If multiple frequency LIN messages are used in the system, then the Master node should not interrupt any time from the beginning of the BREAK delimiter to the end of the Sync byte stop bit.

NOTE: The LIN message tolerance for the system needs to be taken into consideration and this time should be added to each end of the region where the new frame may not be detected.

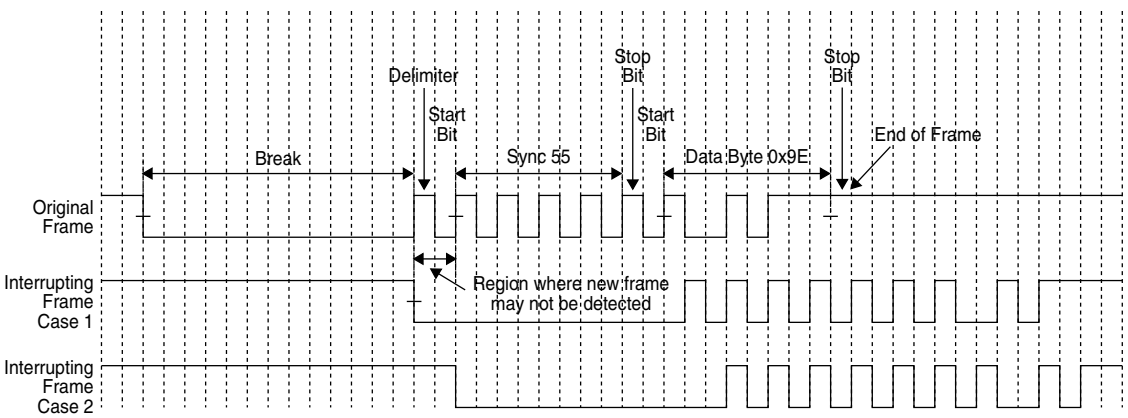

Figure 1. Interrupting frame timing relative to the original frame

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