Mask Set Errata for Mask 0M12J

Introduction

This report applies to mask 0M12J for these products:

- MCF51QE128
- MCF51QE96
- MCF51QE64
- MCF51QE32

SE184-FLVD-STOP3: False low voltage detect when exiting stop3

Errata type:	Silicon
Affected component:	SoC level behavior
Description:	If the low voltage detect (LVD) is enabled (LVDE = 1) but not in stop mode (LVDSE = 0), on some devices the low voltage detect flag (LVDF) will occasionally be set when exiting stop3 mode. If the LVD interrupt is enabled (LVDIE = 1) the interrupt vector will be fetched. If the LVD reset is enabled, the part will reset, and the LVD bit in the System Reset Status (SRS) register will be set. The correct operation of the device is to wake and execute the code immediately after the STOP instruction. If the LVD is not enabled (LVDE = 0) or if LVD is also enabled during stop mode (LVDSE = 1) then this issue will not occur. If the LVD is enabled during stop mode the stop3 current will increase.
Workaround:	A software level change to reliably eliminate the issue is to use only the LVD interrupt (LVDE = 1, LVDIE = 1, and LVDRE = 0). Inside the LVD interrupt service routine, a short state of health check can be made to verify the supply level before proceeding. In this routine, the LVDF should be cleared and then read to determine whether a true low voltage event is present. If the LVDF is set when it is read, then a true LVD condition exists and the MCU can be reset by forcing the execution of an illegal op-code.

SE159-WAIT: Unexpected WAIT mode recovery from STOP mode recovery requests

Errata type: Silicon

Affected component: PMC

Description: If the device is in WAIT mode expecting an enabled interrupt to wakeup the processor to RUN mode, STOP mode recovery request logic from a peripheral that is not configured to wakeup the processor from WAIT mode can unexpectedly trigger a return to RUN mode without there being an enabled interrupt to process.

Workaround: none

SE157-ADC-INCORRECT-DATA: Boundary case may result in incorrect data being read in 10- and 12-bit modes

Errata type: Silicon

Affected component: ADC

Description: In normal 10-bit or 12-bit operation of the ADC, the coherency mechanism will freeze the conversion data such that when the high byte of data is read, the low byte of data is frozen, ensuring that the high and low bytes represent result data from the same conversion.

In the errata case, there is a single-cylce (bus clock) window per conversion cycle when a high byte may be read on the same cycle that subsequent a conversion is completing. Although extremely rare due to the precise timing required, in this case, it is possible that the data transfer occurs, and the low byte read may be from the most recently completed conversion.

In systems where the ADC is running off the bus clock, and the data is read immediately upon completion of the conversion, the errata will not occur. Also, in single conversion mode, if the data is read prior to starting a new conversion, then the errata will not occur.

The errata does not impact 8-bit operation.

Introducing significant delay between the conversion completion and reading the data, while a following conversion is executing/pending, could increase the probability for the errata to occur. Nested interrupts, significant differences between the bus clock and the ADC clock , and not handling the result register reads consecutively, can increase the delay and therefore the probability of the errata occuring.

Workaround: Using the device in 8-bit mode will eliminate the possibility of the errata occuring.

Using the ADC in single conversion mode, and reading the data register prior to initiating a subsequent conversion will eliminate the possibility of the errata occuring.

Minimizing the delay between conversion complete and processing the data can minimize the risk of the errata occuring. Disabling interrupts on higher priority modules and avoiding nested interrupts can reduce possible contentions that may delay the time from completing a conversion and handling the data. Additionally, increasing the bus frequency when running the ADC off the asynchronous clock, may reduce the delay from conversion complete to handling of the data.

SE156-ADC-COCO: COCO bit may not get cleared when ADCSC1 is written to

Errata type: Silicon

Affected component: ADC

Description: If an ADC conversion is near completion when the ADC Status and Control 1 Register (ADCSC1) is written to (i.e., to change channels), it is possible for the conversion to complete, setting the COCO bit, before the write instruction is fully executed. In this scenario, the write may not clear the COCO bit, and the data in the ADC Result register (ADCR) will be that of the recently completed conversion.

If interrupts are enabled, then the interrupt vector will be taken immediately following the write to the ADCSC1 register.

Workaround: It is recommended when writing to the ADCSC1 to change channels or stop continuous conversion, that you write to the register twice. The first time should be to turn the ADC off and disable interrupts, and the second should be to select the mode/channel and re-enable the interrupts.

SE153-CFV1-Interrupted: CFV1 is Interrupted Immediately After Entering Stop Mode

Errata type: Silicon

Affected component: SIM

Description: When an interrupt request coincides with the execution of a stop instruction, the CPU can abort its entry into stop mode, but the SIM continues stop mode processing and shuts down clocks. Extra clocks to the CPU/RAM but not to the Flash lead to a bad read of the interrupt vector from the Flash and an illegal opcode reset.

Workaround: None

SE141-DEBUG: Debug Trace Captures Incorrect Data on Access Errors

Description: Memory referencing operations that are targeted for debug trace data capture but receive an access error on their memory reference incorrectly perform the debug trace data capture. This puts corrupt information in the trace buffer. The trace buffer should not capture information from memory accesses that receive access error

Workaround: Do not have debug trace information capture enabled for accesses to memory locations that might fault.

or

Do not depend on the content of the trace buffer for information captured on an access error.

Note first that the default ColdFire V1 configuration responds to any access error by causing a reset.

Also note that, in general, access errors are not recoverable. It is believed that this behavior will not adversely affect debug.

SE140-MEMORY: Certain Read Memory Instructions Incorrectly Update Target Register and Condition Codes on Access Errors

Description: Certain cases of memory read instructions that receive an access error on their read operation incorrectly update their target register. This corrupts the content of this register, which should be unchanged by a memory read operation that receives an access error. The condition codes affected by these instructions are also incorrectly updated.

The problem instructions are mov.b, mov.w, mvz.b, mvz.w, mvs.b, mvs.w, tst.b, and tst.w.

Workaround: Do not use these instructions to access memory locations that might fault.

or

Do not depend on the content of the target register or condition codes immediately after these instructions receive an access error.

Note first that the default ColdFire V1 configuration responds to any access error by causing a reset.

Also note that, in general, read access errors are not recoverable. It is believed that most software currently follows the second workaround and just aborts the faulting software module or resets on an access error. Very specific software modules that disable resetting on access errors to size memory, check for existing peripherals, or some

SE139-TPM: Incorrect 16-Bit Write to 16-Bit TPM Registers via BDM Single Step

Description: Due to an integration error between the ColdFire V1 BDM access and TPM coherency mechanism, if a user conducts BDM single stepping through software that executes 16-bit writes to 16-bit TPM registers (TPMxMOD and TPMxCxV), reading back the registers will show an invalid value. The read will show that only the data associated with the low byte of the TPM register was written correctly and the high byte remains unchanged. This issue occurs only in BDM mode, therefore 16-bit writes to any 16-bit TPM register (TPMxMOD or TPMxCxV) in user mode will be valid.

Workaround: Executing 8-bit writes to appropriate high and low registers of 16-bit TPM registers (TPMxMODH, TPMxMODL, TPMxCxVH, and TPMxCxVl) will avoid the errata in BDM mode.

Another workaround is for the user to set a breakpoint after the 16-bit TPM registers and run the software to the breakpoint. This method does not require a software change for debugging.

SE138-ICS: Limited ICS Frequency Range When High Range DCO Selected

Errata type: Silicon

Affected component: ICS

Description: In some cases, when the high range DCO is selected, the ICSOUT frequency cannot be trimmed to all frequencies in the specified 48–50.33 MHz range. When the issue occurs, the ICSOUT frequency will default to a higher

frequency, typically above the 50.33 MHz maximum for the device. The issue typically occurs when the reference frequency is trimmed for a 48–49 MHz ICSOUT.

Workaround: When a 32768 Hz reference is used, either by trimming the internal reference or using an external clock, this issue has not been observed. Using this frequency as the reference clock allows proper operation of the DCO in high range. The ICSOUT in this case will be 50.33 MHz.

SE120-IIC: Incorrect Clocking in 10-Bit Addressing Mode

Errata type: Silicon

Affected component: IIC

Description: This erratum is relevant only for applications using 10-bit addressing mode and does not affect 7-bit addressing mode operations.

When hexidecimal values E0,E1,E4,E5,E8,E9,EC,ED,F0,F2,F4, or F6 are used as data in master receive slave transmissions from the IIC module using 10-bit addresses, the IIC clock may produce an incorrect number of pulses. This will result in IIC communication errors.

Workaround: Avoid using the values listed in the erratum description as data in any master receive slave transmission from the IIC module while in 10-bit addressing mode.

SE118-RTC: LPO Enabled in Stop Modes When RTC is in Reset State

Errata type: Silicon

Affected component: RTC

Description: The RTC module comes out of reset with the low power oscillator (LPO) as the selected clock source (RTCLKS = 0:0), but with the RTC module itself disabled (RTCPS = 0:0:0:0). This configuration signals the LPO to be enabled in all modes including stop2 and stop3.

This results in higher than expected stop currents due to the LPO stop mode current adder.

Workaround: To disable the LPO when not needed in the stop modes, set the RTCLKS bits in the RTCSC register to any value other than 0:0. This will select an alternative clock source for the RTC, either the external clock (ERCLK) or the internal clock (IRCLK). Unlike the LPO, the RTC module does not automatically enable either of these clocks to run in stop modes. ERCLK or IRCLK enable is determined by other MCU control bits, not the RTC's. Before entering stop mode, one period of the LPO must expire after setting the RTCLKS bits to ensure that the change has been processed.

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