Mask Set Errata for Mask 0N47T

This report applies to mask 0N47T for these products:
• S32K144

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
e10658	ADC: Trigger loss is not reported
e6939	Core: Interrupted loads to SP can cause erroneous behavior
e9004	Core: ITM can deadlock when global timestamping is enabled
e9005	Core: Store immediate overlapping exception return operation might vector to incorrect interrupt
e6940	Core: VDIV or VSQRT instructions might not complete correctly when very short ISRs are used
e10573	CSEc: FCSESTAT EDB bit is not set correctly in SWD debug mode
e10570	FMC: Potential flash controller hang with multiple flash access errors
e10364	LPI2C: LPI2C sends a STOP condition if transmit FIFO is empty on the completion of a master-receive transfer
e10752	LPI2C: Slave Busy Flag may incorrectly read as zero when 10-bit address mode enabled in slave mode.
e10792	LPI2C: Slave Transmit Data Flag may incorrectly read as one when TXCFG is zero.
e10655	LPSPI: Module Busy Flag may incorrectly read as zero in Master mode
e10527	LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters
e10656	LPUART: The RXD Pin Active Edge Interrupt flag does not assert when an active edge is detected
e10716	RTC: Timer Alarm Flag can assert erroneously
e10777	SCG: Corrupted status when the system clock is switching.

Table 2. Revision History

Revision	Changes
09/15/2016	Initial revision

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Table 2.   Revision History (continued)

Revision	Changes
10/11/2016	The following errata were revised. • e10570
17/feb/2017	The following errata were added. • e10656 • e10655 • e10658 • e10777 • e10716 • e10792 • e10752

e10658:   ADC: Trigger loss is not reported

Description: A trigger loss will not be reported in the following cases:

1. The time between two consecutive triggers on a trigger input is less than 4 cycles of ADC's Module interface clock.

2. One or multiple triggers come on any input while a trigger either stored or under process for that input in the trigger handler.

3. The trigger on a particular input asserts during the period of end-of-conversion cycle of a conversion initiated from this input.

- In these cases the Error in Multiplexed Trigger Request (ADC_SC2[TRGSTERR]) bit in the ADC Status and Control Register 2 will not be set.
- For the third case the Trigger status (ADC_SC2[TRGSTLAT]) bit in the ADC Status and Control Register 2 will also not be set.

Workaround: The time between two consecutive triggers on a particular input should be kept more than one ADC conversion time.

e6939:   Core: Interrupted loads to SP can cause erroneous behavior

Description: ARM Errata 752770: Interrupted loads to SP can cause erroneous behavior

This issue is more prevalent for user code written to manipulate the stack. Most compilers will not be affected by this, but please confirm this with your compiler vendor. MQX™ and FreeRTOS™ are not affected by this issue.

Affects: Cortex-M4, Cortex-M4F

Fault Type: Programmer Category B

Fault Status: Present in: r0p0, r0p1 Open.

If an interrupt occurs during the data-phase of a single word load to the stack-pointer (SP/R13), erroneous behavior can occur. In all cases, returning from the interrupt will result in the load instruction being executed an additional time. For all instructions performing an update to the base register, the base register will be erroneously updated on each execution, resulting in the stack-pointer being loaded from an incorrect memory location.

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The affected instructions that can result in the load transaction being repeated are:

1) LDR SP,[Rn],#imm

2) LDR SP,[Rn,#imm]!

3) LDR SP,[Rn,#imm]

4) LDR SP,[Rn]

5) LDR SP,[Rn,Rm]

The affected instructions that can result in the stack-pointer being loaded from an incorrect memory address are:

1) LDR SP,[Rn],#imm

2) LDR SP,[Rn,#imm]!

Conditions:

1) An LDR is executed, with SP/R13 as the destination.

2) The address for the LDR is successfully issued to the memory system.

3) An interrupt is taken before the data has been returned and written to the stack-pointer.

Implications:

Unless the load is being performed to Device or Strongly-Ordered memory, there should be no implications from the repetition of the load. In the unlikely event that the load is being performed to Device or Strongly-Ordered memory, the repeated read can result in the final stack-pointer value being different than had only a single load been performed.

Interruption of the two write-back forms of the instruction can result in both the base register value and final stack-pointer value being incorrect. This can result in apparent stack corruption and subsequent unintended modification of memory.

Workaround: Most compilers are not affected by this, so a workaround is not required.

However, for hand-written assembly code to manipulate the stack, both issues may be worked around by replacing the direct load to the stack-pointer, with an intermediate load to a general-purpose register followed by a move to the stack-pointer.

If repeated reads are acceptable, then the base-update issue may be worked around by performing the stack pointer load without the base increment followed by a subsequent ADD or SUB instruction to perform the appropriate update to the base register.

e9004:   Core: ITM can deadlock when global timestamping is enabled

Description: ARM ERRATA 806422

The Cortex-M4 processor contains an optional Instrumentation Trace Macrocell (ITM). This can be used to generate trace data under software control, and is also used with the Data Watchpoint and Trace (DWT) module which generates event driven trace. The processor supports global timestamping. This allows count values from a system-wide counter to be included in the trace stream.

When connected directly to a CoreSight funnel (or other component which holds ATREADY low in the idle state), the ITM will stop presenting trace data to the ATB bus after generating a timestamp packet. In this condition, the ITM_TCR.BUSY register will indicate BUSY.

Once this condition occurs, a reset of the Cortex-M4 is necessary before new trace data can be generated by the ITM.

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Timestamp packets which require a 5 byte GTS1 packet, or a GTS2 packet do not trigger this erratum. This generally only applies to the first timestamp which is generated.

Devices which use the Cortex-M optimized TPIU (CoreSight ID register values 0x923 and 0x9A1) are not affected by this erratum.

Workaround: There is no software workaround for this erratum. If the device being used is susceptible to this erratum, you must not enable global timestamping.

e9005: Core: Store immediate overlapping exception return operation might vector to incorrect interrupt

Description: ARM Errata 838869: Store immediate overlapping exception return operation might vector to incorrect interrupt

Affects: Cortex-M4, Cortex-M4F

Fault Type: Programmer Category B Rare

Fault Status: Present in: r0p0, r0p1 Open.

The Cortex-M4 includes a write buffer that permits execution to continue while a store is waiting on the bus. Under specific timing conditions, during an exception return while this buffer is still in use by a store instruction, a late change in selection of the next interrupt to be taken might result in there being a mismatch between the interrupt acknowledged by the interrupt controller and the vector fetched by the processor.

Configurations Affected

This erratum only affects systems where writeable memory locations can exhibit more than one wait state.

Workaround: For software not using the memory protection unit, this erratum can be worked around by setting DISDEFWBUF in the Auxiliary Control Register.

In all other cases, the erratum can be avoided by ensuring a DSB occurs between the store and the BX instruction. For exception handlers written in C, this can be achieved by inserting the appropriate set of intrinsics or inline assembly just before the end of the interrupt function, for example:

ARMCC:

...

__schedule_barrier();

__asm{DSB};

__schedule_barrier();

}

GCC:

...

__asm volatile ("dsb 0xf" ::: "memory");

}

e6940:   Core: VDIV or VSQRT instructions might not complete correctly when very short ISRs are used

Description: ARM Errata 709718: VDIV or VSQRT instructions might not complete correctly when very short ISRs are used

Affects: Cortex-M4F

Fault Type: Programmer Category B

Fault Status: Present in: r0p0, r0p1 Open.

On Cortex-M4 with FPU, the VDIV and VSQRT instructions take 14 cycles to execute. When an interrupt is taken a VDIV or VSQRT instruction is not terminated, and completes its execution while the interrupt stacking occurs. If lazy context save of floating point state is enabled then the automatic stacking of the floating point context does not occur until a floating point instruction is executed inside the interrupt service routine.

Lazy context save is enabled by default. When it is enabled, the minimum time for the first instruction in the interrupt service routine to start executing is 12 cycles. In certain timing conditions, and if there is only one or two instructions inside the interrupt service routine, then the VDIV or VSQRT instruction might not write its result to the register bank or to the FPSCR.

Workaround: A workaround is only required if the floating point unit is present and enabled. A workaround is not required if the memory system inserts one or more wait states to every stack transaction.

There are two workarounds:

1) Disable lazy context save of floating point state by clearing LSPEN to 0 (bit 30 of the FPCCR at address 0xE000EF34).

2) Ensure that every interrupt service routine contains more than 2 instructions in addition to the exception return instruction.

e10573:   CSEc: FCSESTAT EDB bit is not set correctly in SWD debug mode

Description: The External Debug status (FCSESTAT[EDB]) bit in the Flash CSEc Status register does not show a connected debugger status if SWD mode is used.

The EDB bit is used to qualify the availability of security keys. In JTAG mode the EDB bit is correctly set.

Workaround: When using SWD debug mode, do not configure keys to be locked when debugger connection is detected.

In order to protect keys disable SWD pins (SWD_DIO and SWD_CLK) by the MUX (PORT_PCR[MUX]) bit in the Pin Control Register at the beginning of software.

e10570:   FMC: Potential flash controller hang with multiple flash access errors

Description: A bus request targeting the PFlash or DFlash Flash Memory Controller (FMC) may result in a system bus hang under the following conditions:

1. The FMC single entry buffer is faulted and invalid

2. The FMC speculation buffer is faulted and valid

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3. A flash request hits in the FMC speculation buffer

If all 3 conditions describe above occur, the system bus request to the flash will result in a hang.

Workaround: Disable the speculation buffer with the On Chip Memory Descriptor in the Miscellaneous Control Module (MSCM_OCMDR0[5]=0b1 and MSCM_OCMDR1[5]=0b1).

e10364:   LPI2C: LPI2C sends a STOP condition if transmit FIFO is empty on the completion of a master-receive transfer

Description: If the transmit FIFO is empty at the end of a master receive transfer and the AUTOSTOP (MCFGR1[AUTOSTOP]) bit in the Master Configuration Register 1 is clear, the LPI2C master sends a STOP condition before the next repeated START condition.

Workaround: Use software or DMA to queue up the subsequent transfer in the transmit FIFO before the completion of the master-receive transfer.

e10752:   LPI2C: Slave Busy Flag may incorrectly read as zero when 10-bit address mode enabled in slave mode.

Description: When operating in slave mode with 10-bit addressing enabled and an address match is detected on the first address byte, the Slave Busy Flag, SSR[SBF], may incorrectly read as zero.

Workaround: When using the LPI2C in slave mode when 10-bit addressing is enabled, and the SSR[SBF] bit is read as a one, then the flag is set. If it is read as a zero, it must be read a second time and this second read will be the correct state of the bit.

e10792:   LPI2C: Slave Transmit Data Flag may incorrectly read as one when TXCFG is zero.

Description: When SCFGR1[TXCFG] = 0, the slave transmit data ready flag can incorrectly assert for one cycle.

Workaround: Set SCFGR1[TXCFG] = 1.

e10655:   LPSPI: Module Busy Flag may incorrectly read as zero in Master mode

Description: When operating in master mode, the Module Busy Flag, SR[MBF], may incorrectly read as zero. This applies only to master mode and not to slave mode.

Workaround: When using the LPSPI in master mode and the SR[MBF] bit is read as a one then the flag is set. If it is read as a zero, it must be read a second time and this second read will be the correct state of the bit.

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e10527: LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters

Description: When the LPUART transmitter is idle (LPUART_STAT[TC]=1), two break characters may be sent when using LPUART_CTRL[SBK] to send one break character. Even when LUART_CTRL[SBK] is set to 1 and cleared (set to 0) immediately.

Workaround: To queue a single break character via the transmit FIFO, set LPUART_DATA[FRETSC]=1 with data bits LPUART_DATA[T9:T0]=0.

e10656: LPUART: The RXD Pin Active Edge Interrupt flag does not assert when an active edge is detected

Description: The RXD Pin Active Edge Interrupt (LPUART_STAT[RXEDGIF]) flag in the LPUART Status Register should set when an active edge is detected and the Receiver Enable (LPUART_CTRL[RE]) bit in the LPUART Control Register is set. However, the LPUART_STAT[RXEDGIF] flag will only set if the RX Input Active Edge Interrupt Enable (LPUART_BAUD[RXEDGIE]) bit in the LPUART Baud Rate Register is also set. Note that LPUART_BAUD[RXEDGIE] enables the interrupt for the LPUART_STAT[RXEDGIF] flag.

Workaround: Set LPUART_BAUD[RXEDGIE] bit if using the LPUART_STAT[RXEDGIF] flag.

e10716: RTC: Timer Alarm Flag can assert erroneously

Description: Writing to the Time Alarm Register (RTC_TAR) at the same time the RTC Seconds Register is incrementing can assert the Time Alarm Flag (RTC_SR[TAF]) bit in the RTC Status Register.

Workaround: Write the Time Alarm Register (RTC_TAR) when the RTC Seconds Register is not incrementing. This can be when Time Counter Enable (RTC_SR[TCE]) bit in the RTC Status Register is clear or within the RTC_SR[TAF] interrupt routine.

Alternatively, if the RTC_SR[TAF] is asserted following a write to the RTC_TAR, then write the RTC_TAR again.

e10777: SCG: Corrupted status when the system clock is switching.

Description: The SCG_RCCR[SCS] and SCG_HCCR[SCS] may have a corrupted status during the interval when the system clock is switching

Workaround: The SCS field should be read twice by the software to ensure the system clock switch has completed.

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