RAppID–Rapid Application Initialization and Documentation

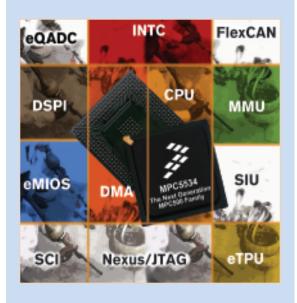### Reduce Development Time!

RAppID is a family of graphical development tools for the MPC5XXX family of PowerPC® controllers that enables the user to quickly and easily configure the controller PLUS generate complete documentation. It can also be used as a learning tool to gain an understanding of the controller and it's peripherals.

RAppID not only generates C code for initializing the registers, but it also provides a system initialization function that brings the controller up in an orderly sequence.

Use RAppID to save time and become an expert on the MPC5XXX Family.

Initialization Is Just a Click Away… Envision, Configure, Build

Product Highlights

- Intuitive, easy-to-use graphical user interface (GUI)
- Comprehensive initialization of the CPU, memory and peripherals
- Automatic DMA register setting from peripherals for basic modes
- Built-in consistency checks to minimize incorrect settings
- Automatic report generation of settings
- Efficient C and assembly code generation for compilers from companies such as Wind River®, Green Hills® and Freescale
- ANSI- or MISRA-compliant code and supporting header files
- Online documentation and built-in tool tips
- Provisions for revision management
- Automatic date and time stamps on generated code and reports
- Enhanced register viewer—browse registers by peripheral
- Modular code generation—generate code for any or all peripherals
- Project import/export capability for distributed development teams
- Ability to define multiple initialization strategies and chose either runtime or compile time for execution
- Full eTPU host initialization and code image download
- Ability to register custom eTPU functions and assign channels
- Wizards for eMIOS initialization and function settings

System Requirements

- Microsoft Windows NT, 2000 or XP
- 512 MB RAM recommended
- Minimum 1 GHz processor recommended
- Standard screen resolutions supported

Order information

VG-RAPPID-5554SW
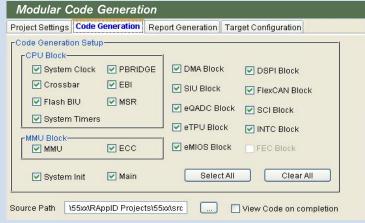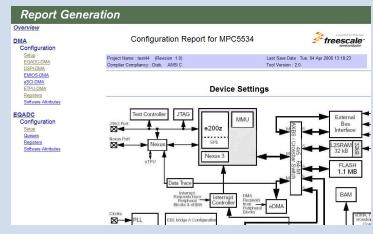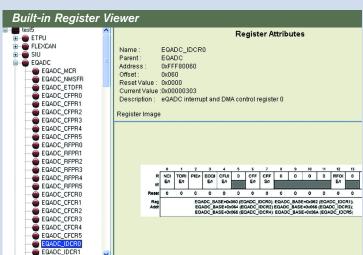VG-RAPPID-5553SW
VG-RAPPID-5534SW (supports both 5533/5534)

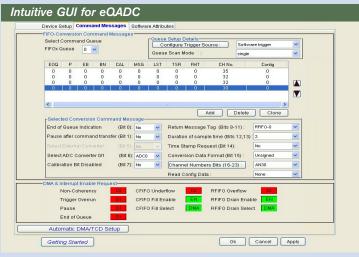For future part numbers, contact your Freescale sales representative.

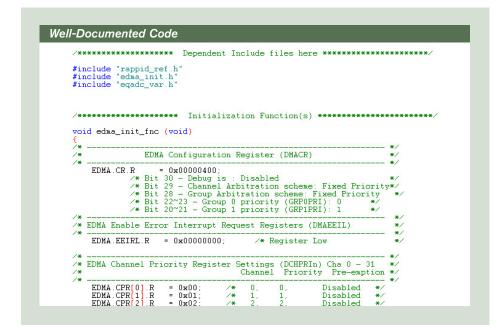**freescale**™
semiconductor

RAppID… Initialization is Just a Click Away!

Modular Code Generation

Project Settings | **Code Generation** | Report Generation | Target Configuration

Code Generation Setup

CPU Block
- ☑ System Clock
- ☑ PBRIDGE
- ☑ Crossbar
- ☑ EBI
- ☑ Flash BIU
- ☑ MSR
- ☑ System Timers

- ☑ DMA Block
- ☑ DSPI Block
- ☑ SIU Block
- ☑ FlexCAN Block
- ☑ eQADC Block
- ☑ SCI Block
- ☑ eTPU Block
- ☑ INTC Block
- ☑ eMIOS Block
- ☐ FEC Block

MMU Block
- ☑ MMU
- ☑ ECC

- ☑ System Init
- ☑ Main

[Select All] [Clear All]

Source Path \55xx\RAppID Projects\55xx\src [...] ☐ View Code on completion

Report Generation

Overview

DMA
Configuration
- Setup
- EQADC-DMA
- DSPI-DMA
- EMIOS-DMA
- eSCI-DMA
- ETPU-DMA
- Registers
- Software Attributes

EQADC
Configuration
- Setup
- Queues
- Registers
- Software Attributes

Configuration Report for MPC5534

| Project Name : test44   (Revision :1.0) | Last Save Date : Tue, 04 Apr 2006 13:18:23 |
| Complier Compliancy : Diab,   ANSI C | Tool Version : 2.0 |

Device Settings

Built-in Register Viewer

test5
- ETPU
- FLEXCAN
- SIU
- EQADC
  - EQADC_MCR
  - EQADC_NMSFR
  - EQADC_ETDFR
  - EQADC_CFPR0
  - EQADC_CFPR1
  - EQADC_CFPR2
  - EQADC_CFPR3
  - EQADC_CFPR4
  - EQADC_CFPR5
  - EQADC_RFPR0
  - EQADC_RFPR1
  - EQADC_RFPR2
  - EQADC_RFPR3
  - EQADC_RFPR4
  - EQADC_RFPR5
  - EQADC_CFCR0
  - EQADC_CFCR1
  - EQADC_CFCR2
  - EQADC_CFCR3
  - EQADC_CFCR4
  - EQADC_CFCR5
  - EQADC_IDCR0
  - EQADC_IDCR1

Register Attributes

Name :   EQADC_IDCR0
Parent :   EQADC
Address :   0xFFF80060
Offset :   0x060
Reset Value : 0x0000
Current Value :0x00000303
Description : eQADC interrupt and DMA control register 0

Register Image

EQADC_BASE+0x060 (EQADC_IDCR0); EQADC_BASE+0x062 (EQADC_IDCR1);
EQADC_BASE+0x064 (EQADC_IDCR2) EQADC_BASE+0x066 (EQADC_IDCR3);
EQADC_BASE+0x068 (EQADC_IDCR4) EQADC_BASE+0x06A (EQADC_IDCR5);

Intuitive GUI for eQADC

Device Setup | **Command Messages** | Software Attributes

FIFO-Conversion Command Messages

Select Command Queue
FIFOx Queue 0

Queue Setup Details
[Configure Trigger Source :] Software trigger
Queue Scan Mode : single

EOQ	P	EB	BN	CAL	MSG	LST	TSR	FMT	CH No.	Config
0	0	0	0	0	0	0	0	0	35	0
0	0	0	0	0	0	0	0	0	32	0
0	0	0	0	0	0	0	0	0	32	0
0	0	0	0	0	0	0	0	0	30	0

[Add] [Delete] [Clone]

Selected Conversion Command Message

End of Queue Indication (Bit 0): No	Return Message Tag (Bits 8-11) : RFIFO-0
Pause after command transfer (Bit 1): No	Duration of sample time (Bits 12,13) : 2
Select External Converter (Bit 5): No	Time Stamp Request (Bit 14): No
Select ADC Converter 0/1 (Bit 6): ADC0	Conversion Data Format (Bit 15): Unsigned
Calibration Bit Disabled (Bit 7): No	Channel Numbers Bits (16-23): AN30
	Read Config Data : None

DMA & Interrupt Enable Request

Non-Coherency	DI	CFIFO Underflow	DI	RFIFO Overflow	DI
Trigger Overrun	DI	CFIFO Fill Enable	EN	RFIFO Drain Enable	EN
Pause	DI	CFIFO Fill Select	DMA	RFIFO Drain Select	DMA
End of Queue	DI				

[Automatic DMA/TCD Setup]

[Getting Started]   [Ok] [Cancel] [Apply]

Well-Documented Code

```
/******************  Dependent Include files here ***********************/

#include "rappid_ref.h"
#include "edma_init.h"
#include "eqadc_var.h"


/******************  Initialization Function(s) ************************/

void edma_init_fnc (void)
{
/* ----------------------------------------------------------------- */
/*              EDMA Configuration Register (DMACR)                  */
/* ----------------------------------------------------------------- */
    EDMA.CR.R   = 0x00000400;
            /* Bit 30 - Debug is : Disabled                */
            /* Bit 29 - Channel Arbitration scheme: Fixed Priority*/
            /* Bit 28 - Group Arbitration scheme: Fixed Priority  */
            /* Bit 22~23 - Group 0 priority (GRP0PRI): 0        */
            /* Bit 20~21 - Group 1 priority (GRP1PRI): 1        */
/* ----------------------------------------------------------------- */
/* EDMA Enable Error Interrupt Request Registers (DMAEEIL)           */
/* ----------------------------------------------------------------- */
    EDMA.EEIRL.R  = 0x00000000;    /* Register Low          */

/* ----------------------------------------------------------------- */
/* EDMA Channel Priority Register Settings (DCHPRIn) Cha 0 - 31      */
/* ----------------                    Channel  Priority  Pre-emption */
/* ----------------------------------------------------------------- */
    EDMA.CPR[0].R  = 0x00;   /*  0,    0,        Disabled  */
    EDMA.CPR[1].R  = 0x01;   /*  1,    1,        Disabled  */
    EDMA.CPR[2].R  = 0x02;   /*  2,    2,        Disabled  */
```

What our Customers are saying about RAppID:

"I have ported code to new processors many times, and I have to admit that this one is going very smoothly, thanks to the tool that automates a lot of tedious tasks, letting the user concentrate on the important things."

"You are doing a good job."

— A Global Tier 1 Software Engineer

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