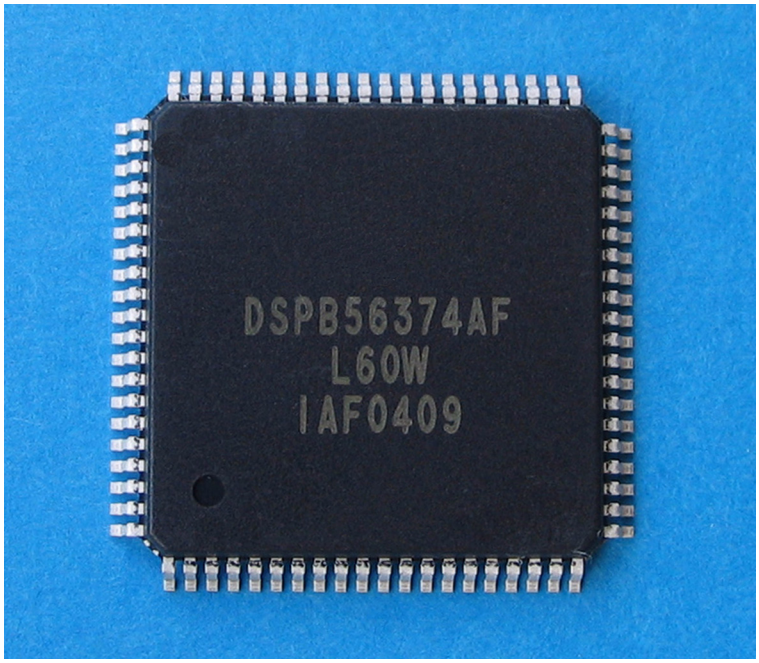
Product Brief

24-Bit Audio Digital Signal Processor



Significant architectural enhancements include:

- a barrel shifter
- 24-bit addressing
- patch module
- direct memory access (DMA)

The DSP56374 is available in either a 52-pin or 80-pin TQFP at 150 million instructions per second (MIPS) using an internal 150 MHz clock at 1.25 V.

Overview

The DSP56374 is designed to support a multitude of digital signal processing applications requiring a lot of horsepower in a small package. While the DSP56374 is designed with flexibility and thus is versatile in the types of applications it can support, it does include a powerful set of audio features, including various built-in audio peripherals and embedded software designed to meet the needs of both consumer and automotive audio applications.

The DSP56374 provides a wealth of audio processing functions including an operating system, various equalization algorithms, compression, signal generator, tone control, fade/balance, level meter/spectrum analyzer, and many more. The DSP56374 also supports various matrix decoders and sound field processing algorithms.

The DSP56374 uses the high performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs), combined with the audio signal processing capability of the Freescale Symphony™ DSP family. This design provides a two-fold performance increase over Freescale's popular DSP56000 core family of DSPs while retaining code compatibility.

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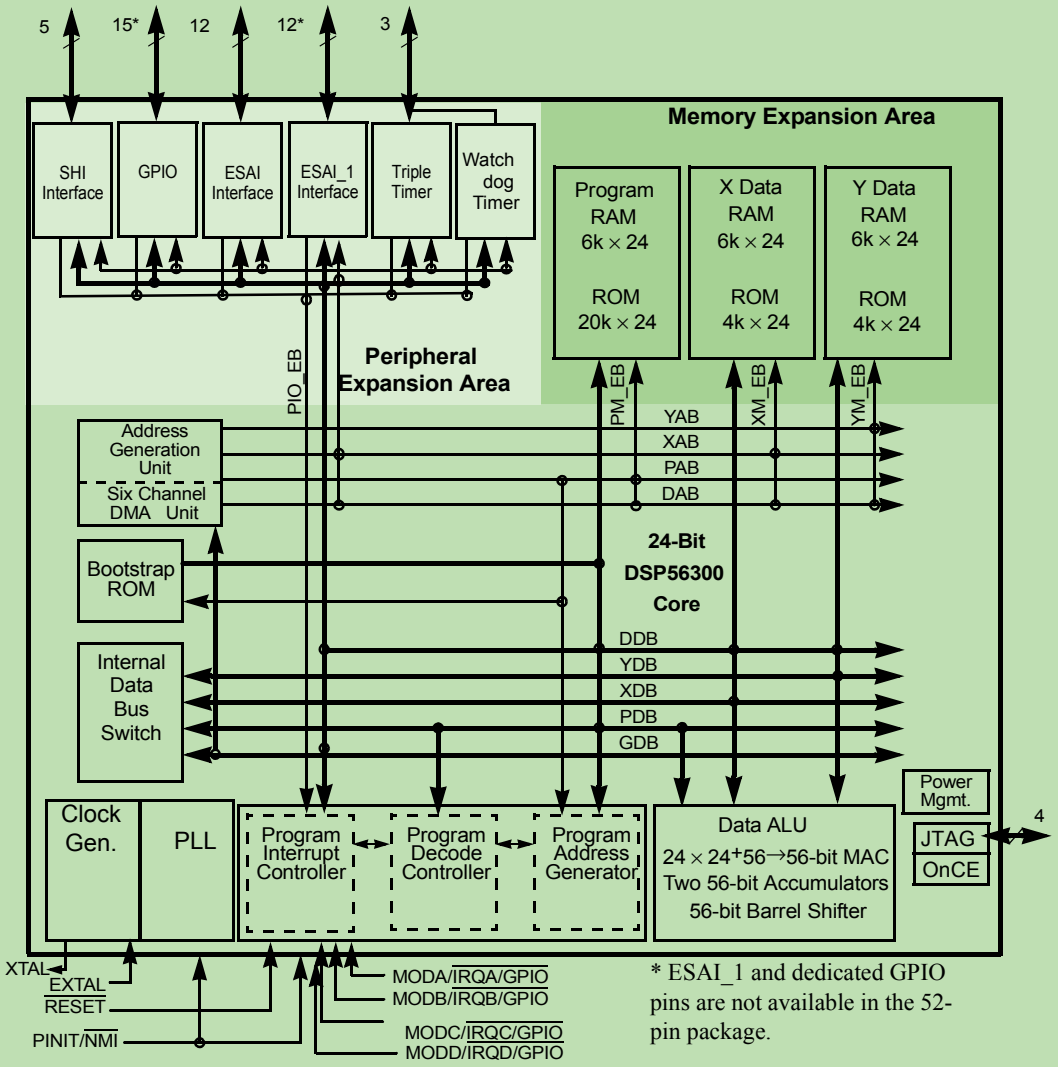
Block Diagram



* ESAI_1 and dedicated GPIO pins are not available in the 52-pin package.

On-Chip Memory Confirguration

> 6K x 24 Bit Y-Data RAM and 4K x 24 Bit Y-Data ROM
> 6K x 24 Bit X-Data RAM and 4K x 24 Bit X-Data ROM
> 6K x 24 Bit Program RAM
> 20K x 24 Bit Program and Bootstrap ROM including a PROM-patching mechanism
> Various memory switches are available. See memory table below.

Bit Settings			Memory Sizes (24-bit words)					
MSW1	MSW0	MS	Prog RAM	X Data RAM	Y Data RAM	Prog ROM	X Data ROM	Y Data ROM
X	X	0	6K	6K	6K	20K	4K	4K
0	0	1	2K	10K	6K	20K	4K	4K
0	1	1	4K	8K	6K	20K	4K	4K
1	0	1	8K	4K	6K	20K	4K	4K
1	1	1	10K	4K	4K	20K	4K	4K

Peripheral modules

- Enhanced Serial Audio Interface (ESAI): up to four receivers and up to six transmitters, master or slave I^2S, Sony, AC97, network and other programmable protocols
- Enhanced Serial Audio Interface I (ESAI_1): up to 4 receivers and up to 6 transmitters, master or slave. Supports I^2S, Sony, AC97, network and other programmable protocols. Note: for 80-pin package only.
- Serial Host Interface (SHI): SPI and I^2C protocols, 10-word receive FIFO, support for 8, 16 and 24-bit words.
- Triple Timer module (TEC)
- Hardware Watchdog Timer
- Most pins of unused peripherals may be programmed as GPIO lines. Up to 47 pins can be configured as GPIO on the 80-pin package, and up to 20 pins on the 52-pin package.

DSP Modular Chassis

- 1.25 V core with a 3.3 V peripheral I/O
- 150 Million Instructions Per Second (MIPS) with a 150 MHz clock at an internal logic supply (QVDDL) of 1.25 V (0°C to 70°C for consumer-grade devices; -40°C to 85 °C for automotive-grade devices)
- Object Code-Compatible with the 56K core
- Data ALU with a 24 x 24 bit multiplier-accumulator and a 56-bit barrel shifter, and 16-bit arithmetic support
- Program Control with position independent code support and instruction cache support
- Six-channel DMA controller
- Low jitter, PLL-based clocking with a wide range of frequency multiplications (1 to 1024), predivider factors (1 to 32) and power-saving clock divider (2^i: i=0 to 7). Reduces clock noise.
- Internal address tracing support and OnCE for hardware/software debugging
- JTAG port
- Very low-power CMOS design, fully static design with operating frequencies down to DC
- STOP and WAIT low-power standby modes

DSP56374 Documentation

This table lists the documents that provide a complete description of the DSP56374 and are required to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or through the Freescale DSP home page on the Internet (the source for the latest information).

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56300FM
DSP56374 User Guide	Detailed description of the 56374 24-bit digital signal processor (DSP), its memory, operating modes, and peripheral modules	DSP56374UG
DSP56374 Technical Data Sheet	Detailed description of timing, voltage level and temperature related specifications.	DSP56374

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DSP56374PB
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