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QorIQ LS1021A Family Communications Processor Product Brief

Contents

1 Overview

This document provides an overview of the features and functionality of the LS1021A integrated processor family.

The LS1021A family consists of the following three primary part numbers:

- LS1020A: Targeted at the enterprise or consumer grade networking and router applications
- LS1021A: Targeted at the industrial automation, printing and military/aerospace markets
- LS1022A: Targeted at low-power demanding applications

All three parts feature dual 32-bit ARM® Cortex®-A7 processors, each with 32 KB of instruction and data L1 cache, as well as 512 KB of shared, coherent L2 cache, and the ARM CCI400 interconnect bus. Each of the products in the LS1021A family offers an optimized blend of system logic, performance and power utilization required for Internet of Things (IoT), networking, Machine to Machine (M2M), telecommunications, industrial automation and general embedded applications.

Some of the outstanding features the LS1021A family are:

- A cost-effective, power efficient and highly integrated system-on-chip design that extends the reach of NXP's Value Performance line of QorIQ communications processors.

- Delivers greater performance levels than any prior sub-3W (typical) processor.
- Features dual 32-bit Cortex v7 cores running at up to 1.2 GHz and yielding over 7,000 Coremarks.
- Offers an integrated LCD controller (featured on the LS1021A), together with upgraded high-speed interfaces, including support for DDR3L/4 running at up to 1600 MHz as well as Super Speed USB3.0 and SATAIII.

The LS1021 and LS1020 both feature an integrated 4-lane, 6 GHz multi-protocol SerDes that can support up to two SGMII Gigabit Ethernet ports, PCIe 2.0 in x1, x2 or x4 configurations, or the single SATAIII controller. The integrated super speed USB3.0 PHY features a dedicated SerDes.

The LS1021A processor sets a new standard for power efficiency, delivering over 7,000 Coremarks of performance at under 3.7 watts total SOC power. This highly efficient performance is coupled with an outstanding array of protocol and latest generation interface support, including:

- Dual high-performance ARM Cortex-A7 cores featuring ECC protected L1 and L2 caches
- DDR3L/4 memory controller that supports up to 1,600 Mtps, with optional ECC support
- Dual PCI Express 2.0 controllers
- SATAIII
- Twin USB controllers (one USB3.0 with integrated PHY, together with a separate USB2.0 controller)
- Three enhanced triple speed Gigabit Ethernet controllers with support for MII, RGMII, and SGMII, as well as IEEE 1588

The LS1021A and LS1020A both feature a hardware-based security acceleration engine for secure networking, as well as support for secure boot and ARM TrustZone and NXP's QorIQ TrustArchitecture.

Multicore processing support:

Both ARM Cortex-A7 cores can operate in symmetric multiprocessing mode (SMP) to achieve higher performance, or they can run in asymmetric processing mode (AMP) with each core supporting independent operating systems, and performing separate tasks. For example, one core can manage data plane tasks, while the other supports tasks in the control plane. This flexibility enables application developers to assign distinct processing resources to distinct tasks that need guaranteed performance.

2 Use cases

LS1021A is a highly versatile and power-efficient chip that can be configured to meet a wide variety of applications. This section provides several use cases that can be supported by LS1021A.

2.1 Multi-protocol IoT gateway

This figure shows the chip supporting a multi-protocol IoT gateway. Point-to-point broadband gateways can be used for copper, wireless, or fiber-to-the-home applications that use different optical connectors for Fiber WAN interface transceivers. With this technology, ISPs and Telcos (operators and carriers) can offer greater bandwidth over greater distances to deliver IPTV or home entertainment services to end customers.

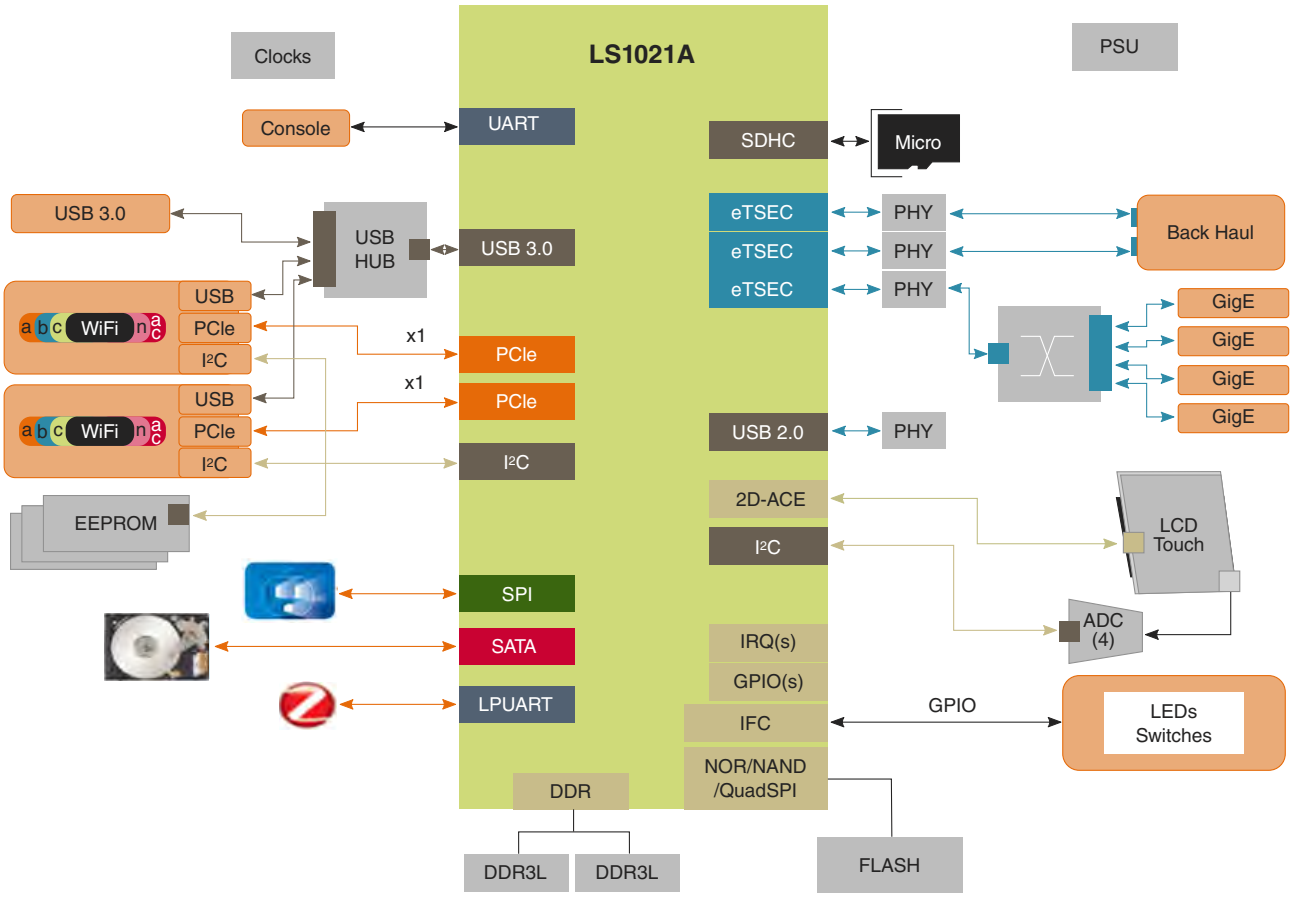

Figure 1. Multi-protocol IoT gateway

2.2 Mobile wireless gateway

The increasing adoption of Wi-Fi in practically all mobile devices, including laptops, PCs, tablets, smart phones, and e-readers has promoted transport operators to make Wi-Fi service available on airliners and trains, as well as cruise ships, and will soon include interstate and metro mass transit operators. To support broadband connectivity for the mobile Wi-Fi network, service providers are utilizing 4G or LTE cellular, as well as satellite uplink for off-shore or locations where cellular network coverage is not available.

The following are advantages of LS1021A for mobile wireless gateway application:

- Scalable dual-core ARM® Cortex®-A7 cores support newest generation of 802.11ac Wi-Fi radios and a wide range of services/applications
- Extreme efficiency of ARM Cortex-A7 cores delivers extending performance capabilities for next generation 802.11ac
- Dual PCIe Gen 2 controllers to support dual band 802.11ac and 802.11n WLAN networks
- USB 3.0 support for LTE/4G wireless broadband backhaul
- SATA to support high speed data streaming
- SD/MMC enables configuration or storage
- Optional LCD controller enables touchscreen display for configuration and diagnostics

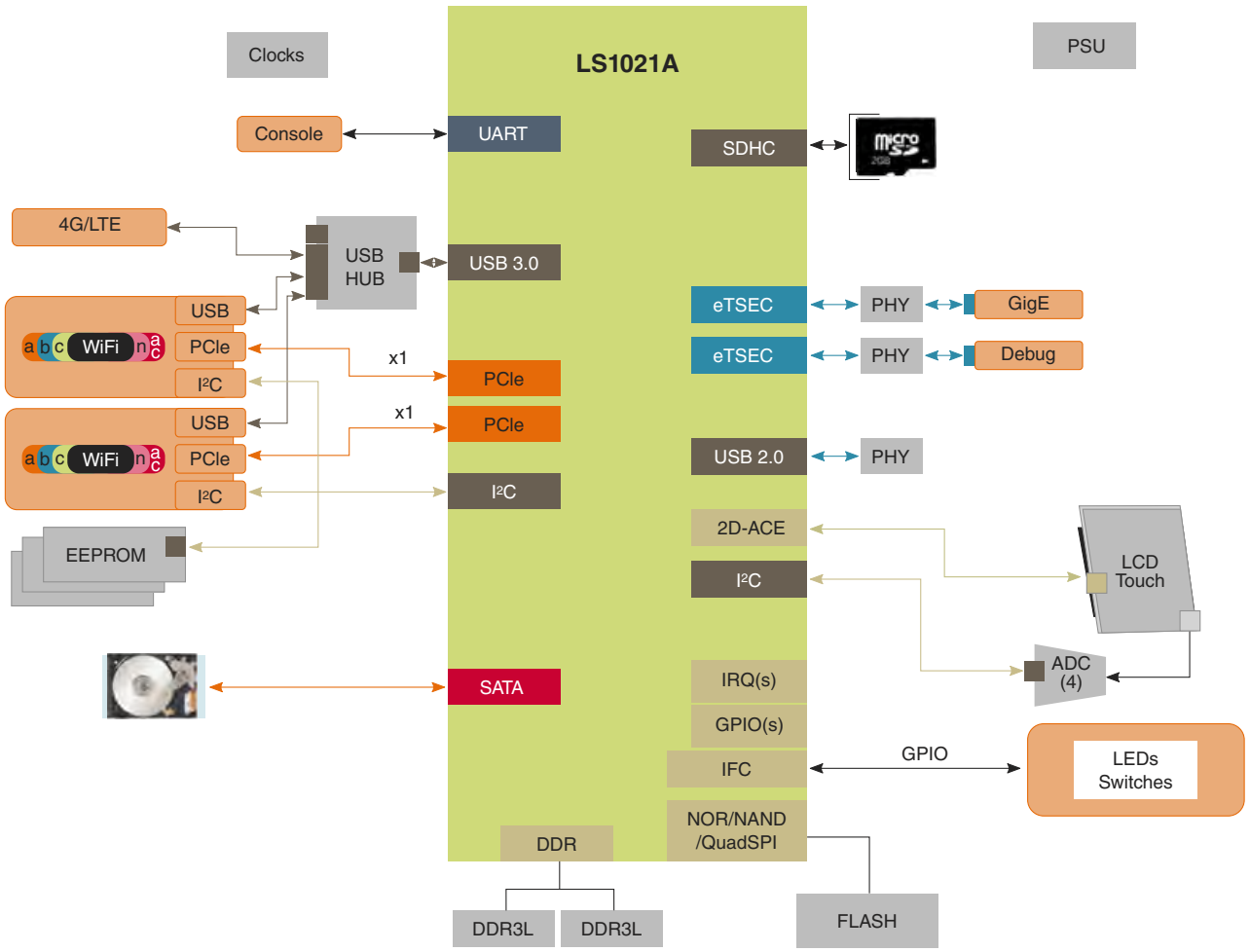

Figure 2. Mobile wireless gateway with optional touchscreen LCD

2.3 Enterprise access point WLAN

This figure shows LS1021A acting as a full function Enterprise access point to support next generation 802.11ac wireless LAN networks.

The chip provides following advantages:

- Scalable dual-core ARM® Cortex®-A7 cores support newest generation of 802.11ac Wi-Fi radios and a wide range of services/applications
- Extreme efficiency of ARM Cortex-A7 cores delivers extending performance capabilities of current power over Ethernet (POE) applications
- Dual PCIe Gen 2 controllers support dual band radio applications
- Support for low power DDR4 memory, as well as DDR3L at up to 1.6 MT/s for outstanding performance
- Integrated security processor supports the full range of Ethernet and Wi-Fi security protocols
- Trust Architecture as well as ARM TrustZone are supported

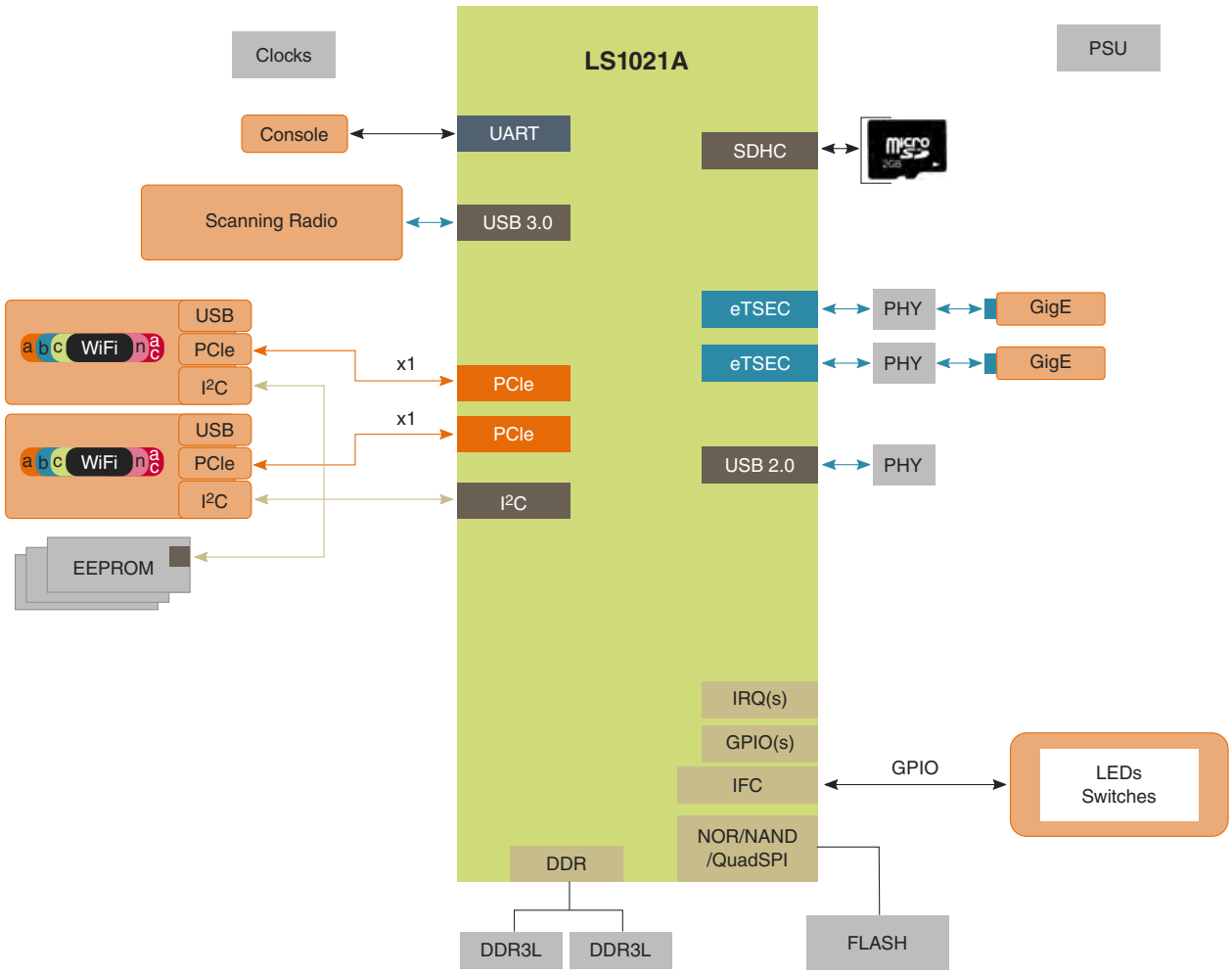

Figure 3. Enterprise access point WLAN

2.4 Industrial/factory automation controller

The chip has following advantages:

- Scalable dual-core ARM® Cortex®-A7 cores support a wide range of industrial or factory automation applications
- Advanced security and trust architecture
- Complete range of industrial connectivity
- High-performance ASIC expansion interface
- QUICC Engine support for UART (ProfiBus)
- Dual PCIe Gen 2 controllers
- High-performance integrated flash controller (IFC) ASIC expansion interface advanced security and trust architecture

The following figure shows that LS1021A has the interfaces required for almost all industrial / factory automation applications.

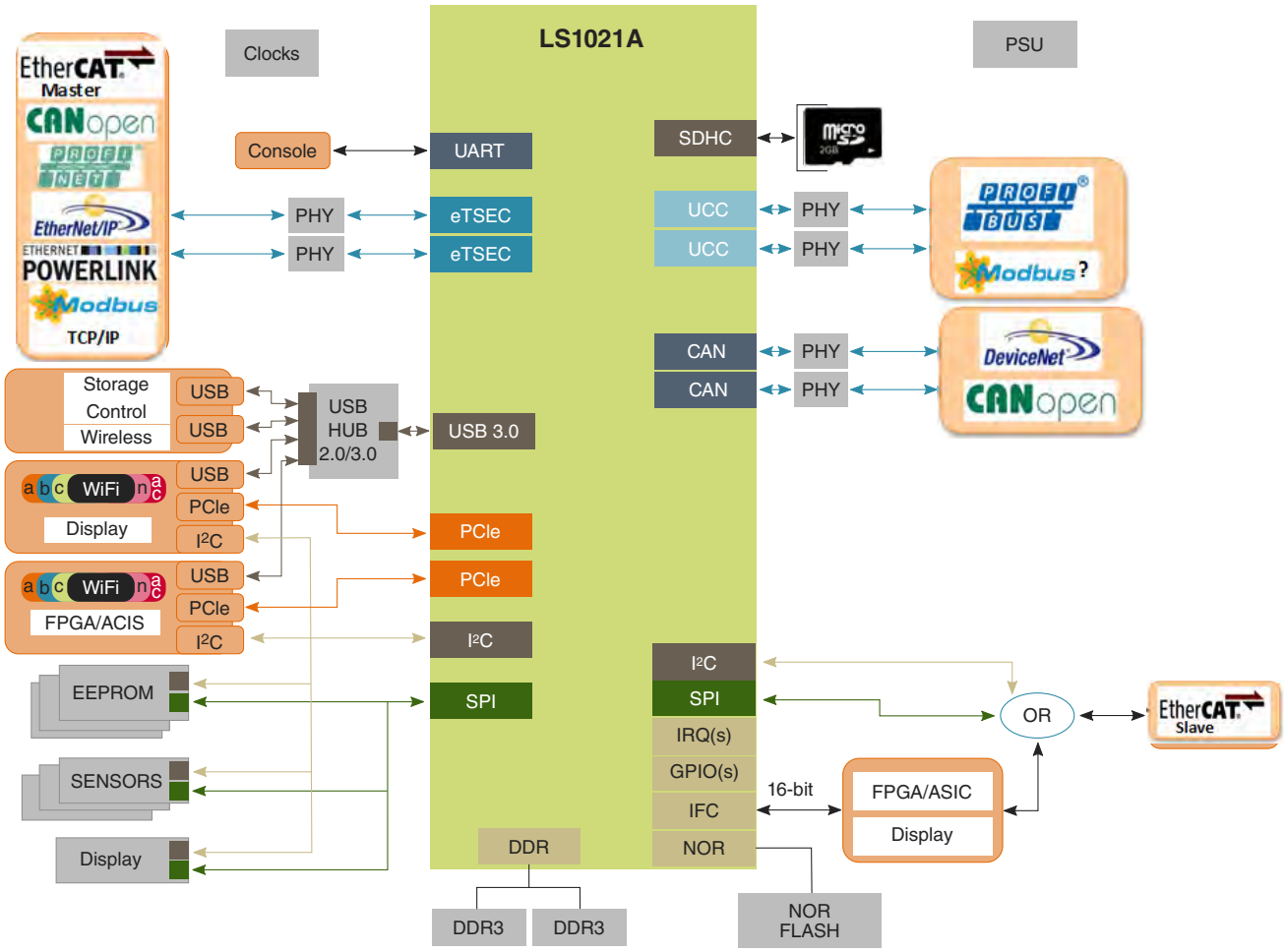

Figure 4. Industrial/factory automation controller

2.5 Printing

Followings are advantages of LS1021A for printer application:

- Scalable dual-core ARM® Cortex®-A7 processors to support wide-range of services/applications
- PCIe Gen2.0 for high bandwidth connectivity to print/scan ASICs
- USB 3.0 super-speed support for ultra-fast data transfer
- High-bandwidth wireless for un-tethered location flexibility
- Cloud connectivity for real-time feedback/control and content delivery
- Display controller for touch-screen-based UI interface support

The following figure shows LS1021A use case for low and mid-range MFP printer designs.

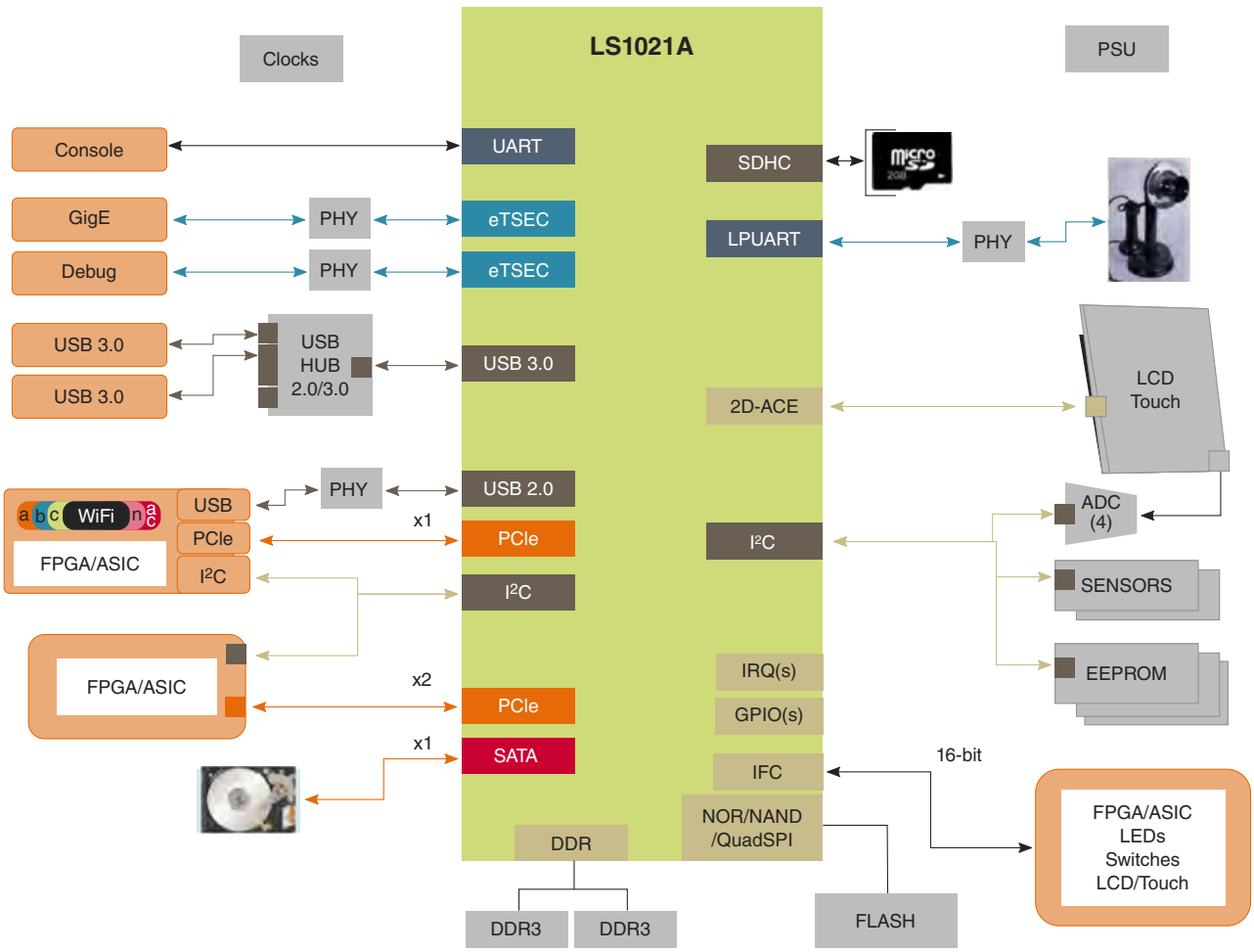

Figure 5. MFP printer application

2.6 SOHO / low-end branch router

This figure shows LS1021A in an all-in-one router solution with integrated wired, wireless and services into a single platform. Services, such as Voice over IP (VoIP), video on demand (VoD), WAN acceleration, security, wireless, monitoring and management can be supported.

Followings are advantages LS1021A for this application:

- Scalable dual-core processor to support wide-range of services/applications
- Advanced security and trust architecture
- Datapath architecture to offload packet processing
- Support for legacy T1/E1, ISDN and IP services

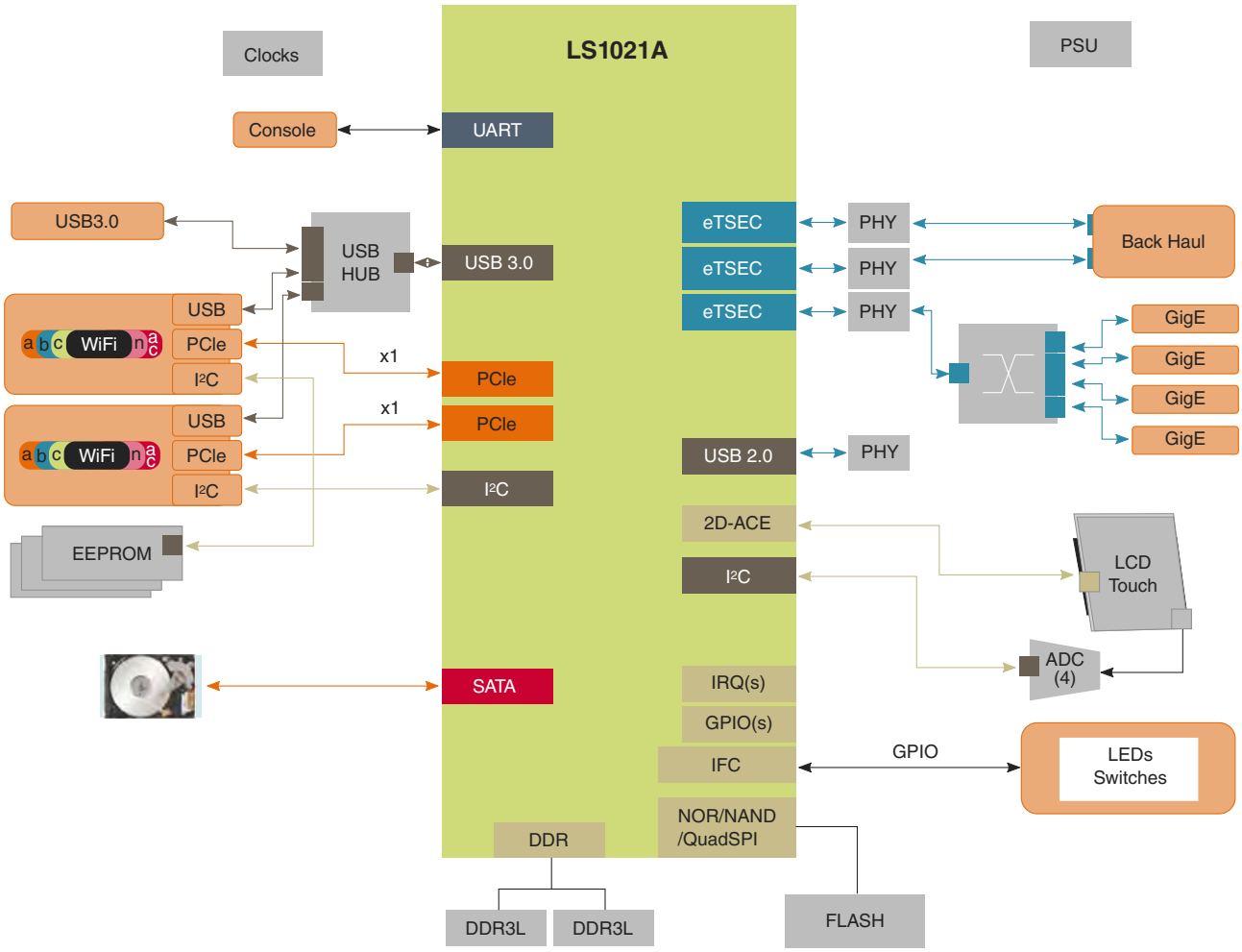

Figure 6. SOHO / low-end branch router

3 Chip-level features

Key features of LS1021A include:

- Dual ARM® Cortex®-A7 cores, running at up to 1.2 GHz with 32 KB instruction and 32 KB data caches, and ECC single bit error detect and single bit correction, and Neon module support
- 512 KB coherent L2 cache with ECC single bit error detect and single bit correction
- 32/16/8-bit DDR3L/4 supporting up to 1600 Mtps
- ARM Core-Link CCI-400 Cache Coherent Interconnect
- 3x enhanced triple speed Gb Ethernet controllers, with IEEE 1588 support
  - IPv6 forwarding at 2 Gbps
  - MII, RGMII, SGMII
- Security offload engine
  - IPSec forwarding at up to 1 Gbps
- 4-lane 6 GHz SerDes
- 2x PCI Express 2.0 5 GT/s signaling technology
  - 1-lane, 2-lane or 4-lane

- 1x USB3.0 controller with integrated PHY - 5 GT/s super speed signaling rate
- 1x USB2.0 controller with ULPI
- 1x SATA 3.0 – 6 GT/s
- LCD controller with support for up to 4 planes
- Integrated Flash Controller
- Quad SPI NAND/NOR Flash
- 2x DUART
- 6x Low Power UART
- Power consumption less than 3.7 W (worst case thermal design power)
- 28-nm HPM process technology
- Operating junction temperature (Tj) rang 0-125C and -40-125C (industrial specification)

3.1 Block diagram

This figure shows the major functional units within the LS1021A chip.

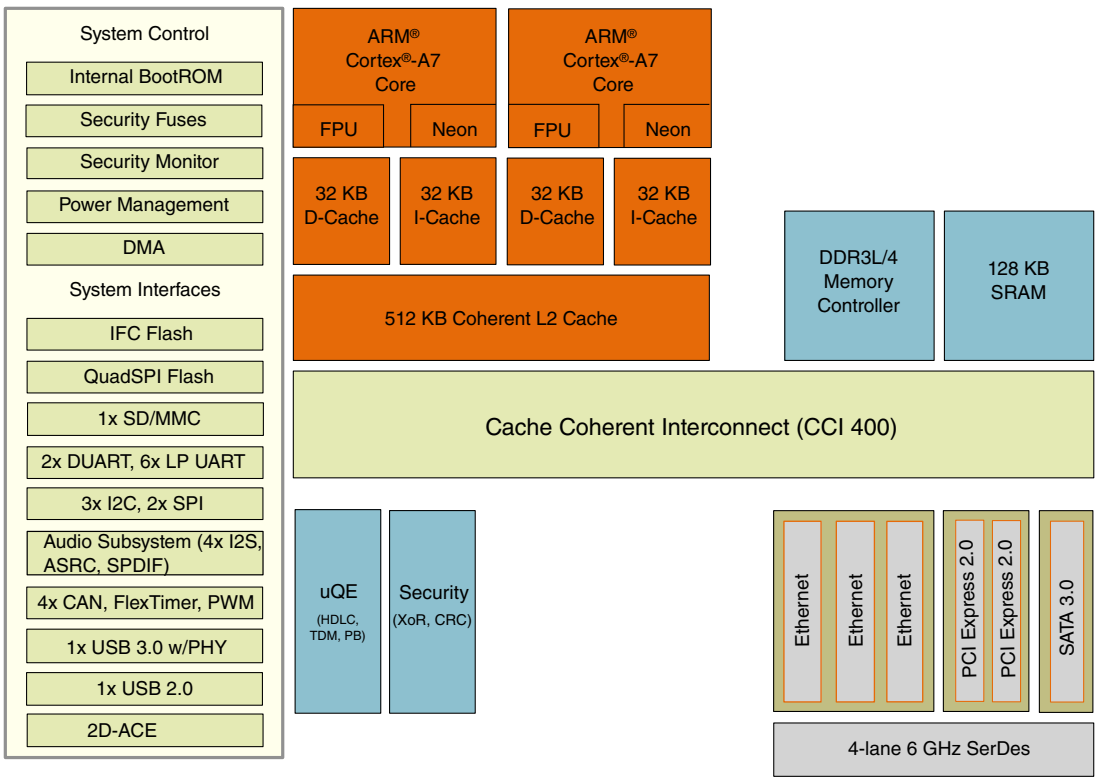

Figure 7. Block diagram

3.2 ARM® Cortex®-A7 core

The chip features two high-performance Cortex-A7 cores:

- 40-bit large physical address extensions (LPAE)
- 8-stage in order pipeline with partial dual issue capability and predictive branch detection.
- DSP and NEON SIMD extensions onboard (per core)
- VFPv4 floating point unit onboard (half-, single- and double-precision)

- NEON technology to accelerate multimedia and signal processing algorithms
- Hardware virtualization support
- Embedded trace macrocell and coresight design kit for unobtrusive tracing of instruction execution and data access
- 32 KB data + 32 KB instruction L1 cache per core with ECC protection (single-bit ECC correction is always enabled and is handled silently)
- Integrated low-latency high bandwidth level-2 cache controller, supporting 512 KB shared L2 cache with ECC (single-bit ECC correction is always enabled and is handled silently)
    - 8-way set associative cache with sequential TAG and data RAM access
    - Automatic data prefetching into L2 cache for load streaming
    - MP support:
        - Four independent tag banks handle multiple requests in parallel
        - Integrated snoop control unit into L2 pipeline
        - Direct data transfer line migration supported from CPU to CPU

3.3 ARM CoreLink cache coherent interconnect (CCI-400)

The CCI-400 combines interconnect and coherency functions into a single module. The CCI-400 is an infrastructure component that supports:

- Data coherency between both Cortex-A7 cores and all I/O masters with three independent Points-of-Serialization (PoS) and full barrier support high-bandwidth, cross-bar interconnect functionality between the masters and up to three slaves
- DVM message transport between masters
- Quality-of-Service (QoS) regulation for shaping traffic profiles
- Performance monitoring unit (PMU) to count performance-related events
- Programmers view (PV) to control the coherency and interconnect functionality

3.4 DDR memory controllers

The DDR memory controller supports DDR3L and DDR4 SDRAM. The memory interface controls main memory accesses and supports a maximum of 32 GB of main memory. The chip supports chip-select interleaving within the controller.

The DDR memory controller can be configured to retain the currently active SDRAM page for pipelined burst accesses. Page mode support of up to 64 simultaneously open pages can dramatically reduce access latencies for page hits. Using ECC, the chip detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble.

In addition, the DDR controller offers an initialization bypass feature for use by system designers to prevent reinitialization of main memory during system power-on after an abnormal shutdown. The DDR controller also supports active zeroization of system memory upon detection of a user-defined security violation.

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3.6 Integrated security engine (SEC)

The security engine (SEC 5.5) is designed to support Secure Boot, ARM TrustZone as well as Trust Architecture. The modular and scalable SEC 5.5 supports booting to a known good state (secure boot) with untamperable boot code, key storage, IO protection, and secure debug.

The SEC 5.5 security engine can process all algorithms associated with IPSec, IKE, SSL/TLS, iSCSI, SRTP, IEEE Std 802.11i™, IEEE Std 802.16™ (WiMAX), and IEEE Std 802.1AE™ (MACSec).

Also, the SEC 5.5 is optimized to perform multi-algorithmic operations (for example, 3DES-HMAC-SHA-1) in a single pass of the data.

Key features and functions supported by the SEC 5.5 security engine include the following:

- XOR engine for parity checking in RAID storage applications
- Four crypto-channels, each supporting multi-command descriptor chains
- Cryptographic execution units:
    - PKHA - Public Key Hardware Accelerator
    - DESA - Data Encryption Standard Accelerator
    - AESA - Advanced Encryption Standard Accelerator
    - MDHA - Message Digest Hardware Accelerator
    - CRCA - Cyclical Redundancy Check Accelerator
    - RNG - Random Number Generator

3.7 Universal Serial Bus (USB) controller and PHY

The USB controller provides point-to-point connectivity conforming to the Universal Serial Bus revision specification. The USB controller and integrated PHY can be configured to operate as a stand-alone host, stand-alone device, or with both host and device functions operating simultaneously.

The host and device functions are configured to support the following types of USB transfers:

- Bulk
- Control
- Interrupt
- Isochronous

Key features of the USB controller include the following:

- Supports OTG 2.0
- USB dual-role operation and can be configured as host or device
- Supports operation as a stand-alone USB device
    - Supports one upstream facing port
    - Supports four programmable bidirectional USB endpoints
- Supports operation as a stand-alone USB host controller
    - Supports USB root hub with one downstream-facing port
    - Enhanced host controller interface (EHCI) compatible
- Super-speed (5 Gbit/s), High-speed (480 Mbit/s), and full-speed (12 Mbit/s) operations

3.7.1 USB 2.0 controller and ULPI interface

Key features of the USB 2.0 controller include the following:

- Complies with USB specification, Rev. 2.0
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- Both controllers support operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI)-compatible
- controller supports operation as a stand-alone USB device
  - Support one upstream-facing port
  - Support six programmable USB endpoints

3.7.2 USB 3.0 controller and PHY

Key features of the USB 3.0 controller include the following:

- OTG 2.0
- USB dual-role operation and can be configured as host or device
- Operation as a stand-alone USB device
  - One upstream facing port
  - Six programmable USB endpoints
- Operation as a stand-alone USB host controller
  - USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Super-speed (5 GT/s), High-speed (480 Mbps), and full-speed (12 Mbps) operations.

NOTE

Super-speed operation in host mode is not supported when it is configured as OTG 2.0.

3.8 High speed I/O interfaces

The chip supports the SGMII, PCI Express 2.0 controller, and SATA high-speed I/O interface standards.

3.8.1 Serial ATA (SATA) controller

The key features of the SATA controller are as follows:

- Single SATA controller with chip-level interface
- Asynchronous notification, hot plug
  - Asynchronous signal recovery
  - Link power management
  - Native command queuing
  - Staggered spin-up
  - Port multiplier support
- Support for SATA I, II, and III data rates 1.5 3.0 Gbaud
- Standard ATA master-only emulation
- ATA shadow registers
- SATA superset registers
- SError, SControl, SStatus
- Interrupt driven
- Power management support
- Error handling and diagnostic features

- Far-end/near-end loopback
- Failed CRC error reporting
- Increased ALIGN insertion rates
- Scrambling and CONT override

3.8.2 PCI Express interface

is compatible with the PCI Express Base Specification Revision 3.0. Key features of the PCI Express interface include the following:

- Power-on reset configuration options allow root complex functionality
- The physical layer operates at Gen2 (2.5 or 5 Gbit/s) data rate per lane
- Receive and transmit ports operate independently, with an aggregate theoretical bandwidth of 32 Gbit/s
- x4, x2, and x1 link widths support
- Both 32- and 40-bit addressing and 256-byte maximum payload size
- Full 64-bit decode with 36-bit wide windows
- Inbound INTx transactions
- Message Signaled Interrupt (MSI) transactions

3.8.3 SGMII

The serial gigabit media independent interface (SGMII) is a high-speed interface linking the Ethernet controller with an Ethernet PHY. SGMII uses differential signaling for electrical robustness. Only four signals are required: receive data and its inverse, and send data and its inverse; no clock signals are required.

3.8.4 High-speed interface multiplexing

The table below shows the supported high-speed interface configurations. The desired configuration must be selected at power-on reset.

Table 1. Supported SerDes options

SerDes Lanes				
SRDS_PRTCL_S1[128:135]RCW	1	2	3	4
00	PCI Express 1 (x4)			
80	PCIe#1 (x2)		PCIe#2 (x2)	
10	PCIe#1 (x1)	SATA1	PCIe#2 (x2)	
20	PCIe#1 (x1)	SGMII1	PCIe#2 (x1)	SGMII2
30	PCIe#1 (x1)	SATA1	SGMII1	SGMII2
40	PCIe#1 (x2)		SATA1	SGMII2
50	PCIe#1 (x2)		PCIe#2 (x1)	SGMII2
60	PCIe#1 (x2)		SGMII1	SGMII2
70	PCIe#1 (x1)	SATA1	PCIe#2 (x1)	SGMII2

3.9 QUICC Engine-Lite

Key features of QUICC Engine-Lite include the following:

- Single 32-bit RISC controller for flexible support of communication peripherals
- Serial DMA channel for reception and transmission on all serial channels
- Two UCCs supporting the following interfaces (not all of them simultaneously):
  - Serial
  - UART
  - Asynchronous HDLC (256 Channels) (bit rate up to 2 Mbit/s)
  - TDM interfaces supporting up to 128 QUICC multichannel controller channels

3.10 Enhanced Secure Digital Host Controller and SDIO

Detailed features of the SD/eSDHC/eMMC controller include the following:

- Conforms to the SD host controller standard specification version 3.0
- Compatible with the MMC system specification version 4.5
- Compatible with the SD Memory Card Physical Layer specification version 3.01
- Compatible with the SD - SDIO card specification version 3.0
- Designed to work with eMMC devices as well as SD Memory, SDIO, and SD combo cards and their variants
- Supports SD UHS-1 speed modes

3.11 Two Dimensional Animation and Compositing Engine (2D-ACE)

The two dimensional animation and compositing engine (2D-ACE) is a system master that fetches graphics stored in internal or external memory and displays them on a TFT LCD panel.

Features supported include:

- Double-pumped pixel data for a low-pin count, 12-bit wide DDR pin interface to support up to 24-bit RGB
- Full RGB888 output to TFT LCD panel
- 16 graphics layers, a default background color layer and a cursor layer
- Blending of each pixel using up to 4 source layers dependent on size of panel
- Programmable panel size up to 2032 x 2047 with pixel clock up to 150 MHz (achievable resolution dependent on system bandwidth)
- Gamma correction with 8-bit resolution on each color component
- Safety mode for tagging pixels on highest priority layers
- Dedicated memory blocks to store a cursor and color look up tables (CLUTs)
- Temporal dithering

3.12 Advanced audio

The integrated audio block includes the I2S/SAI module.

4 Revision history

Table 2. Revision history

Rev. number	Date	Substantive change(s)
1	01/2017	• Updated ARM® Cortex®-A7 cores for 1.2 GHz, yielding over 7,000 Coremarks. • Updated the template for NXP • Replaced "Freescale" instances with "NXP"
0	09/2014	Initial release

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