Freescale Semiconductor
Product Brief

MC9S12XS256PB
Rev. 4, 11-Nov-2008

MC9S12XS-Family

Low Cost 16-Bit Microcontroller Family

Covers MC9S12XS256, MC9S12XS128 and MC9S12XS64

Introduction

The new MC9S12XS-Family of 16-Bit micro controllers is a compatible, reduced version of the MC9S12XE-Family. These families provide an easy approach to develop common platforms from low-end to high-end applications, minimizing the redesign of software and hardware.

Targeted at generic automotive applications and slave CAN nodes, some typical examples of these applications are: Body Controllers, Occupant Detection, Door Modules, RKE Receivers, Smart Actuators, Lighting Modules and Smart Junction Boxes amongst many others. For space-constrained applications, these products are also available in die format.

The MC9S12XS-Family retains many of the features of the S12XE-Family including Error Correction Code (ECC) on Flash memory, a separate Data-Flash Module for code or data storage, a Frequency Modulated Locked Loop (IPLL) that improves the EMC performance and a fast ATD converter.

MC9S12XS-Family will deliver 32-Bit performance with all the advantages and efficiencies of a 16-Bit MCU. It will retain the low cost, power consumption, EMC and code-size efficiency advantages currently enjoyed by users of Freescale's existing 16-Bit MC9S12 and S12X MCU families. Like members of other S12X families, the MC9S12XS-Family will run 16-Bit wide accesses without wait states for all peripherals and memories.

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The MC9S12XS-Family will be available in 112-Pin LQFP, 80-Pin QFP and 64-Pin LQFP package options and maintains a high level of pin compatibility with the S12XE-Family. In addition to the I/O ports available in each module, up to 18 further I/O ports are available with interrupt capability allowing Wake-Up from STOP or WAIT modes.

The peripheral set includes MSCAN, SPI, two SCIs, 8-channel Timer, 8-channel PWM and up to 16-channel 12-bit ATD converter.

Software controlled peripheral-to-port routing enables access to a flexible mix of the peripheral modules in the lower pin count package options.

Features

Features of the MC9S12XS-Family are listed here. Please see Table 1 for memory options and Table 2 for the peripheral features that are available on the different family members.

16-Bit CPU12X	• Upward compatible with MC9S12 instruction set • Enhanced indexed addressing • Access to large data segments independent of PPAGE • Note: five Fuzzy instructions are removed (MEM, WAV,WAVR, REV, REVW)
Enhanced Interrupt Module	• Seven levels of nested interrupts • Flexible assignment of interrupt sources to each interrupt level. • External non-maskable high priority interrupt (XIRQ) • The following inputs can act as Wake-up Interrupts – IRQ and non-maskable XIRQ – CAN receive pins – SCI receive pins – Depending on the package option up to 20 pins on ports J, H and P configurable as rising or falling edge sensitive
System Integrity Support	• Power-on reset (POR) • Illegal address detection with reset • Low-voltage detection with interrupt or reset • Computer Operating Properly (COP) watchdog – Configurable as window COP for enhanced failure detection – Can be initialized out of reset using option bits located in Flash • Clock monitor supervising the correct function of the oscillator

Memory Options	• 64K, 128K and 256K byte Flash • Flash General Features – 64 data bits plus 8 syndrome ECC (Error Correction Code) bits allow single bit failure correction and double fault detection – Erase sector size 1024 bytes – Automated program and erase algorithm – Protection scheme to prevent accidental program or erase – Security option to prevent unauthorized access – Sense-amp margin level setting for reads • 4K and 8K byte Data Flash space – 16 data bits plus 6 syndrome ECC (Error Correction Code) bits allow single bit failure correction and double fault detection – Erase sector size 256 bytes – Automated program and erase algorithm • 4K, 8K and 12K byte RAM
Oscillator (OSC_LCP)	• Loop Control Pierce oscillator utilizing a 4MHz to 16MHz crystal – Current gain control on amplitude output – Signal with low harmonic distortion – Low power – Good noise immunity – Eliminates need for external current limiting resistor • Option for full-swing Pierce without internal feedback resistor utilizing a 2MHz to 40MHz crystal. • Transconductance sized for optimum start-up margin for typical crystals
Internally-Filtered Phase-Locked-Loop (IPLL)	• Phase-locked-loop clock frequency multiplier – No external components required – Reference divider and multiplier allow large variety of clock rates – Automatic bandwidth control mode for low-jitter operation – Automatic frequency lock detector – Configurable option to spread spectrum for reduced EMC radiation (frequency modulation)
Clock and Reset Generator (CRG)	• COP watchdog • Real Time Interrupt • Clock Monitor • Fast wake up from STOP in self clock mode for power saving and immediate program execution • System reset generation

Analog-to-Digital Converter (ATD)	• 16-channel, 12-bit Analog-to-Digital converter – 8/10/12 Bit resolution – 3µs, 10-bit single conversion time – Left or right justified result data – External and internal conversion trigger capability – Internal oscillator for conversion in Stop modes – Wake from low power modes on analogue comparison > or <= match – Continuous conversion mode – Multiplexer for 16 analog input channels – Multiple channel scans – Pins can also be used as digital I/O
Timer (TIM)	• 8 x 16-bit channels for input capture or output compare • 16-bit free-running counter with 8-bit precision prescaler • 1 x 16-bit pulse accumulator
Periodic Interrupt Timer (PIT)	• 4 channel x 24-bit modulus down-count timers – Time-out interrupt – Time-out peripheral trigger • Start of timers can be aligned
Real Time Interrupt (RTI)	• Real Time Interrupt for task scheduling purposes or cyclic wake-up • Can be active in Pseudo Stop mode for low power precision timing tasks
Asynchronous Periodic Interrupt (API)	• Low Power wake-up timer – Internal oscillator driving a down counter – Trimmable to +/-10% accuracy across full operating range – Time-out periods range from 0.2ms to ~13s with a 0.2ms resolution
Pulse Width Modulator (PWM)	• Up to 8 channel x 8-bit or 4 channel x 16-bit Pulse Width Modulator – Programmable period and duty cycle per channel – Center- or left-aligned outputs – Programmable clock select logic with a wide range of frequencies

Multi-Scalable Controller Area Networks (MSCAN)	• 1 Mbit per second, CAN 2.0 A, B software compatible module – Standard and extended data frames – 0 - 8 bytes data length – Programmable bit rate up to 1 Mbps • Five receive buffers with FIFO storage scheme • Three transmit buffers with internal prioritization • Flexible identifier acceptance filter programmable as: – 2 x 32-bit – 4 x 16-bit – 8 x 8-bit • Wake-up with integrated low pass filter option • Loop back for self test • Listen-only mode to monitor CAN bus • Bus-off recovery by software intervention or automatically • 16-bit time stamp of transmitted/received messages
Serial Peripheral Interface (SPI)	• Configurable 8 or 16-bit data size • Full-duplex or single-wire bidirectional • Double-buffered transmit and receive • Master or Slave mode • MSB-first or LSB-first shifting • Serial clock phase and polarity options
Serial Communication Interface (SCI)	• Full-duplex or single wire operation • Standard mark/space non-return-to-zero (NRZ) format • Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths • 13-bit baud rate selection • Programmable character length • Programmable polarity for transmitter and receiver • Receive wakeup on active edge • Break detect and transmit collision detect supporting LIN
Background Debug (BDM)	• Background Debug Module (BDM) with single-wire interface – Non-intrusive memory access commands – Supports in-circuit programming of on-chip non-volatile memory – Supports security

Debugger (xDBG)	• Four comparators A, B, C and D to monitor CPU busses – A and C compares 23-bit address bus and 16-bit data bus with mask register – B and D compares 23-bit address bus only – Three modes: simple address/data match, inside address range or outside address range • 64 x 64-bit circular trace buffer to capture change-of-flow addresses or address and data of every access • Tag-type or force-type hardware breakpoint requests
On-Chip Voltage Regulator (VREG)	• Two parallel, linear voltage regulators with bandgap reference • Low-voltage detect (LVD) with low-voltage interrupt (LVI) • Power-on reset (POR) circuit • Low-voltage reset (LVR)
Input/Output	• Up to 91 general-purpose input/output (I/O) pins depending on the package option and 2 input-only pins • Hysteresis and configurable pull up/pull down device on all input pins • Configurable drive strength on all output pins
Package Options	• 112-pin low-profile quad flat-pack (LQFP), 20x20mm, 0.65mm pitch • 80-pin quad flat-pack (QFP), 14x14mm, 0.65mm pitch • 64-pin low-profile quad flat-pack (LQFP), 10x10mm, 0.5mm pitch • Known good die (KGD)
Operating Conditions	• Wide single Supply Voltage range 3.135V to 5.5V at full performance – Separate supply for internal voltage regulator and I/O allow optimized EMC filtering • 40MHz maximum CPU bus frequency • Ambient temperature range –40°C to 125°C • Temperature Options: – –40°C to 85°C – –40°C to 105°C – –40°C to 125°C

Block Diagram

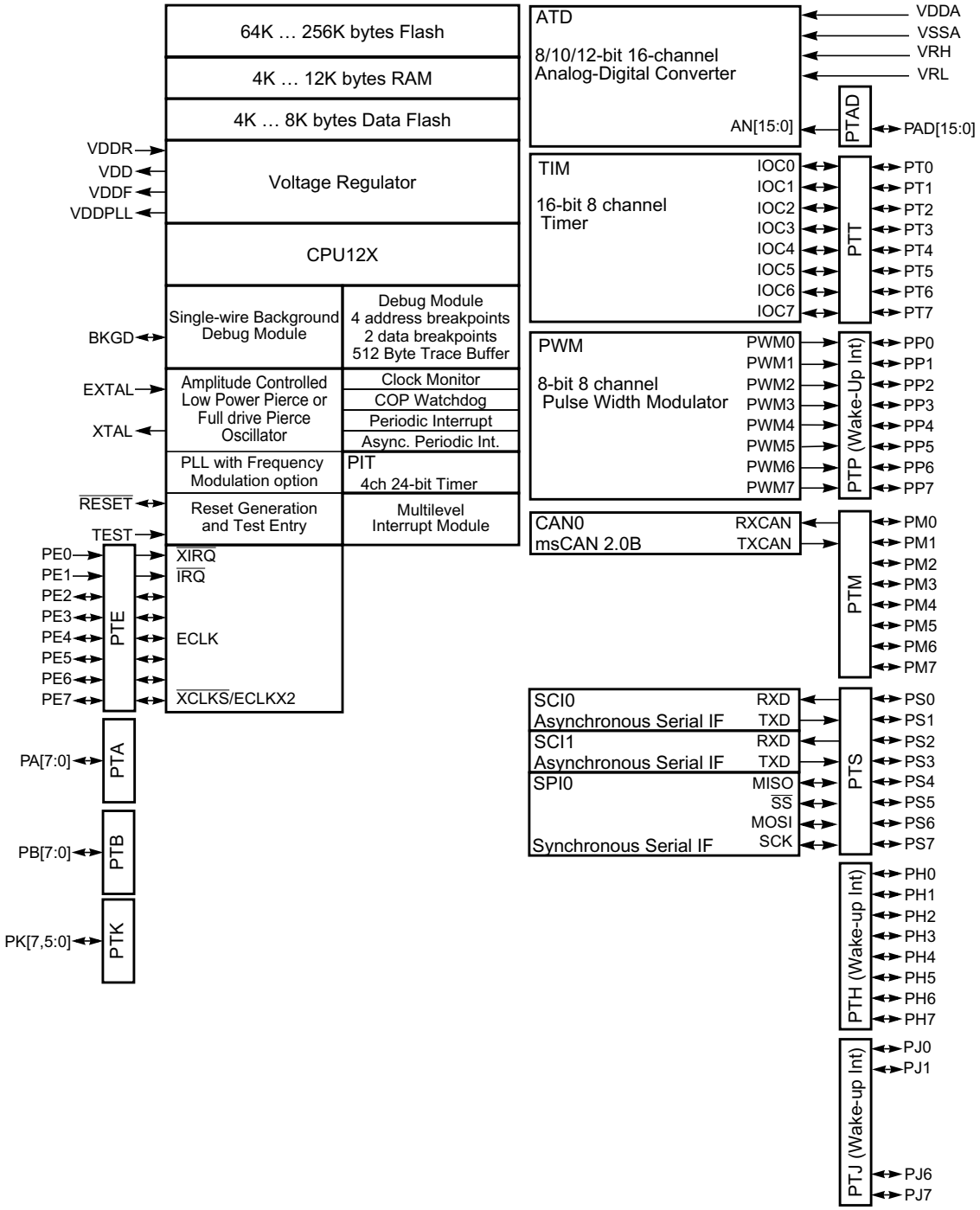

Figure 1. MC9S12XS-Family Block Diagram

Table 1 Package and Memory Options of MC9S12XS-Family

Device	Package	Flash	RAM	Data Flash
9S12XS256	112 LQFP	256K	12K	8K
	80 QFP			
	64 LQFP			
	KGD (Die)			
9S12XS128	112 LQFP	128K	8K	8K
	80 QFP			
	64 LQFP			
	KGD (Die)			
9S12XS64	112 LQFP	64K	4K	4K
	80 QFP			
	64 LQFP			
	KGD (Die)			

Table 2 Peripheral Options of MC9S12XS-Family Members

Device	Package	CAN	SCI	SPI	TIM	PIT	A/D	PWM
9S12XS256	112 LQFP	1	2	1	8ch	4ch	16ch	8ch
	80 QFP	1	2	1	8ch	4ch	8ch	8ch
	64 LQFP	1	2	1	8ch	4ch	8ch	8ch
	KGD (Die)	1	2	1	8ch	4ch	16ch	8ch
9S12XS128	112 LQFP	1	2	1	8ch	4ch	16ch	8ch
	80 QFP	1	2	1	8ch	4ch	8ch	8ch
	64 LQFP	1	2	1	8ch	4ch	8ch	8ch
	KGD (Die)	1	2	1	8ch	4ch	16ch	8ch
9S12XS64	112 LQFP	1	2	1	8ch	4ch	16ch	8ch
	80 QFP	1	2	1	8ch	4ch	8ch	8ch
	64 LQFP	1	2	1	8ch	4ch	8ch	8ch
	KGD (Die)	1	2	1	8ch	4ch	16ch	8ch

NOTE

For the 80QFP and 64LQFP package options, several peripheral functions can be routed under software control to different pins. Not all functions are available simultaneously. For details see Table 4.

Pin Assignments

Table 3 Port Availability by Package Option

Port	112 LQFP	80 QFP	64 LQFP	KGD (Die)
Port AD/ADC Channels	16/16	8/8	8/8	16/16
Port A pins	8	8	4	8
Port B pins	8	8	4	8
Port E pins inc. IRQ/XIRQ input only	8	8	4	8
Port H	8	0	0	8
Port J	4	2	0	4
Port K	7	0	0	7
Port M	8	6	6	8
Port P	8	7	5	8
Port S	8	4	4	8
Port T	8	8	8	8
Sum of Ports	**91**	**59**	**44**	**91**
I/O Power Pairs VDDX/VSSX	2/2	2/2	2/2	2/2

Table 4 Peripheral - Port Routing Options[1]

	SCI1	SPI0	PWM	TIM
PM[1:0]	O			
PM[5:2]		O		
PP[2,0]	O			
PP[2:0]				O
PP[7:4]			X	
PS[3:2]	X			
PS[7:4]		X		
PT[2,0]				X
PT[7:4]			O	

NOTES:
1. “X” denotes reset condition, “O” denotes a possible rerouting under software control

Table 5 Pin-Out Summary[1]

LQFP 112	QFP 80	LQFP 64	KGD (Die)	Pin	2nd Func.	3rd Func.	4th Func.	5th Func.
1	1	1	1	PP3	KWP3	PWM3		
2	2	2	2	PP2	KWP2	PWM2	IOC2	TXD1
3	3	3	3	PP1	KWP1	PWM1	IOC1	
4	4	4	4	PP0	KWP0	PWM0	IOC0	RXD1
5	-	-	5	PK3				
6	-	-	6	PK2				
7	-	-	7	PK1				
8	-	-	8	PK0				
9	5	5	9	PT0	IOC0			
10	6	6	10	PT1	IOC1			

Table 5 Pin-Out Summary[1]

LQFP 112	QFP 80	LQFP 64	KGD (Die)	Pin	2nd Func.	3rd Func.	4th Func.	5th Func.
11	7	7	11	PT2	IOC2			
12	8	8	12	PT3	IOC3			
13	9	9	13	VDDF				
14	10	10	14	VSS1				
15	11	11	15	PT4	IOC4	PWM4		
16	12	12	16	PT5	IOC5	PWM5		
17	13	13	17	PT6	IOC6	PWM6		
18	14	14	18	PT7	IOC7	PWM7		
19	-	-	19	PK5				
20	-	-	20	PK4				
21	-	-	21	PJ1	KWJ1			
22	-	-	22	PJ0	KWJ0			
23	15	15	23	BKGD	MODC			
24	16	16	24	PB0				
25	17	-	25	PB1				
26	18	-	26	PB2				
27	19	-	27	PB3				
28	20	-	28	PB4				
29	21	17	29	PB5				
30	22	18	30	PB6				
31	23	19	31	PB7				
32	-	-	32	PH7	KWH7			
33	-	-	33	PH6	KWH6			
34	-	-	34	PH5	KWH5			
35	-	-	35	PH4	KWH4			
36	24	20	36	PE7	$\overline{\text{XCLKS}}$	ECLKX2		
37	25	-	37	PE6	MODB			
38	26	-	38	PE5	MODA			
39	27	21	39	PE4	ECLK			

Table 5 Pin-Out Summary[1]

LQFP 112	QFP 80	LQFP 64	KGD (Die)	Pin	2nd Func.	3rd Func.	4th Func.	5th Func.
40	28	22	40	VSSX2				
41	29	23	41	VDDX2				
42	30	24	42	$\overline{\text{RESET}}$				
43	31	25	43	VDDR				
44	32	26	44	VSS3				
45	33	27	45	VSSPLL				
46	34	28	46	EXTAL				
47	35	29	47	XTAL				
48	36	30	48	VDDPLL				
49	-	-	49	PH3	KWH3			
50	-	-	50	PH2	KWH2			
51	-	-	51	PH1	KWH1			
52	-	-	52	PH0	KWH0			
53	37	-	53	PE3				
54	38	-	54	PE2				
55	39	31	55	PE1	$\overline{\text{IRQ}}$			
56	40	32	56	PE0	$\overline{\text{XIRQ}}$			
57	41	33	57	PA0				
58	42	34	58	PA1				
59	43	35	59	PA2				
60	44	36	60	PA3				
61	45	-	61	PA4				
62	46	-	62	PA5				
63	47	-	63	PA6				
64	48	-	64	PA7				
65	49	37	65	VDD				
66	50	38	66	VSS2				
67	51	39	67	PAD00	AN00			
68	-	-	68	PAD08	AN08			

Table 5 Pin-Out Summary[1]

LQFP 112	QFP 80	LQFP 64	KGD (Die)	Pin	2nd Func.	3rd Func.	4th Func.	5th Func.
69	52	40	69	PAD01	AN01			
70	-	-	70	PAD09	AN09			
71	53	41	71	PAD02	AN02			
72	-	-	72	PAD10	AN10			
73	54	42	73	PAD03	AN03			
74	-	-	74	PAD11	AN11			
75	55	43	75	PAD04	AN04			
76	-	-	76	PAD12	AN12			
77	56	44	77	PAD05	AN05			
78	-	-	78	PAD13	AN13			
79	57	45	79	PAD06	AN06			
80	-	-	80	PAD14	AN14			
81	58	46	81	PAD07	AN07			
82	-	-	82	PAD15	AN15			
83	59	47	83	VDDA				
84	60	48	84	VRH				
85	61	49	85	VRL[2]				
86	62	49	86	VSSA				
87	-	-	87	PM7				
88	-	-	88	PM6				
89	63	50	89	PS0	RXD0			
90	64	51	90	PS1	TXD0			
91	65	52	91	PS2	RXD1			
92	66	53	92	PS3	TXD1			
93	-	-	93	PS4	MISO0			
94	-	-	94	PS5	MOSI0			
95	-	-	95	PS6	SCK0			
96	-	-	96	PS7	$\overline{SS0}$			
97	67	54	97	TEST				

Table 5 Pin-Out Summary[1]

LQFP 112	QFP 80	LQFP 64	KGD (Die)	Pin	2nd Func.	3rd Func.	4th Func.	5th Func.
98	68	-	98	PJ7	KWJ7			
99	69	-	99	PJ6	KWJ6			
100	70	55	100	PM5	SCK0			
101	71	56	101	PM4	MOSI0			
102	72	57	102	PM3	$\overline{SS0}$			
103	73	58	103	PM2	MISO0			
104	74	59	104	PM1	TXCAN0	TXD1		
105	75	60	105	PM0	RXCAN0	RXD1		
106	76	61	106	VSSX1				
107	77	62	107	VDDX1				
108	-	-	108	PK7				
109	78	63	109	PP7	KWP7	PWM7		
110	-	-	110	PP6	KWP6	PWM6		
111	79	64	111	PP5	KWP5	PWM5		
112	80	-	112	PP4	KWP4	PWM4		

NOTES:
1. Table shows a superset of pin functions. Not all functions are available on all derivatives
2. VRL and VSSA share single pin on 64-pin package option

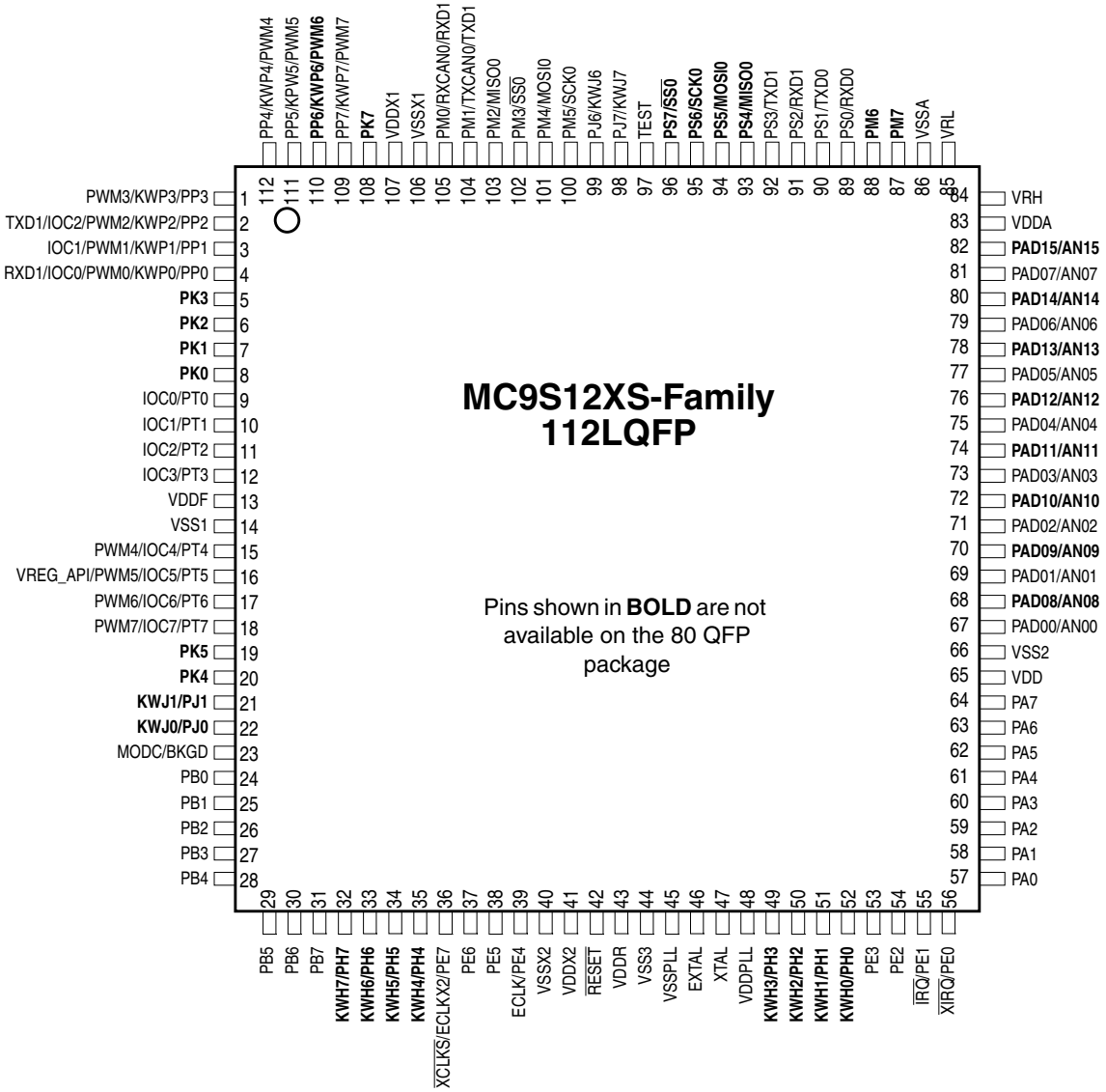

Figure 2. MC9S12XS-Family Pin Assignments 112-pin LQFP Package

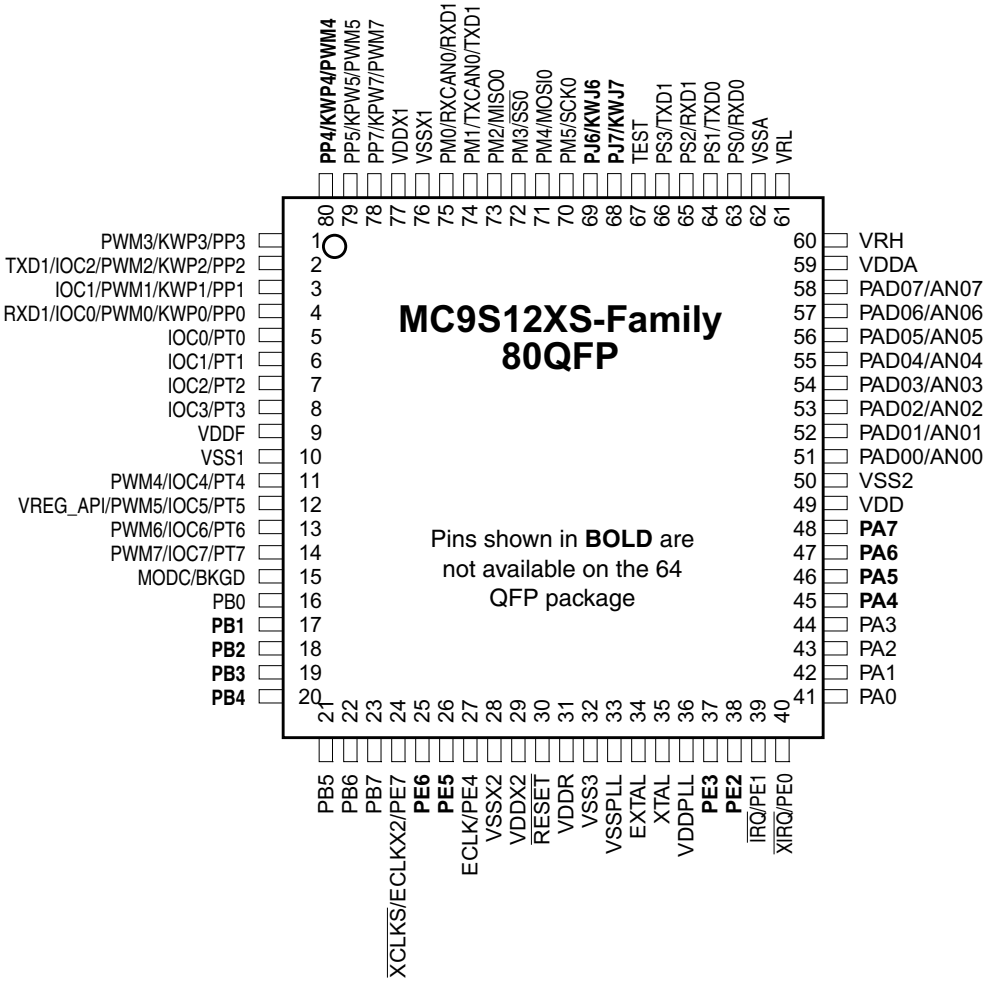

Figure 3. MC9S12XS-Family Pin Assignments 80-pin QFP Package

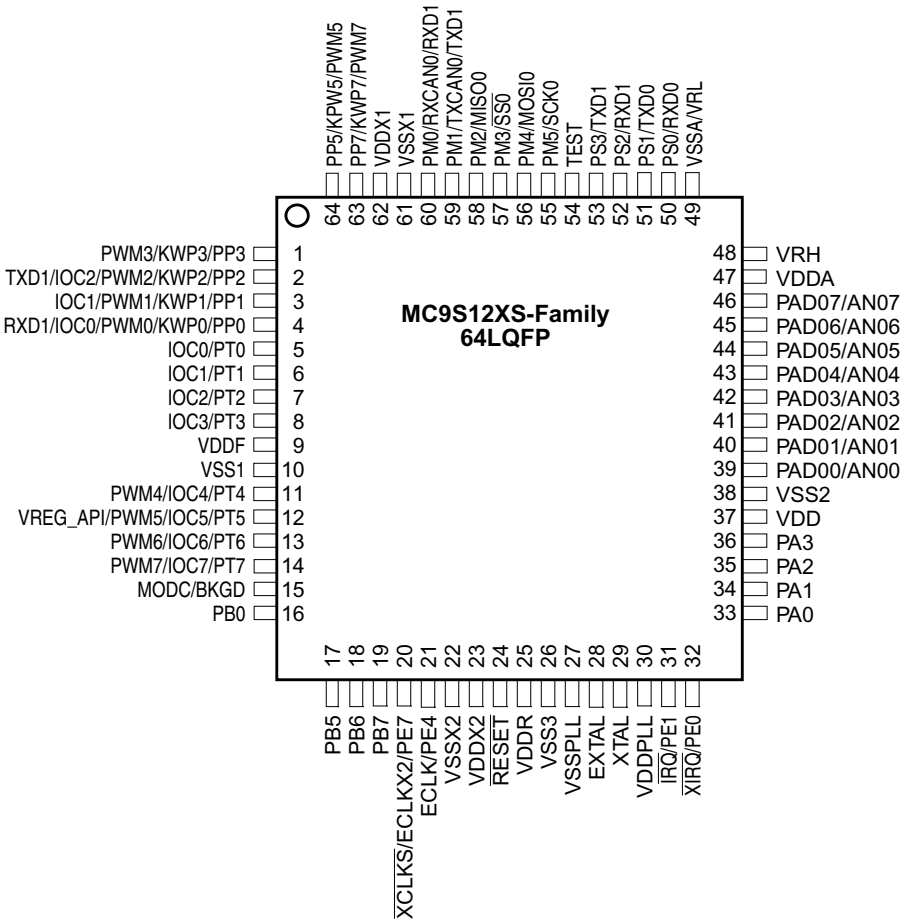

Figure 4. MC9S12XS-Family Pin Assignments 64-pin LQFP Package

Memory Map

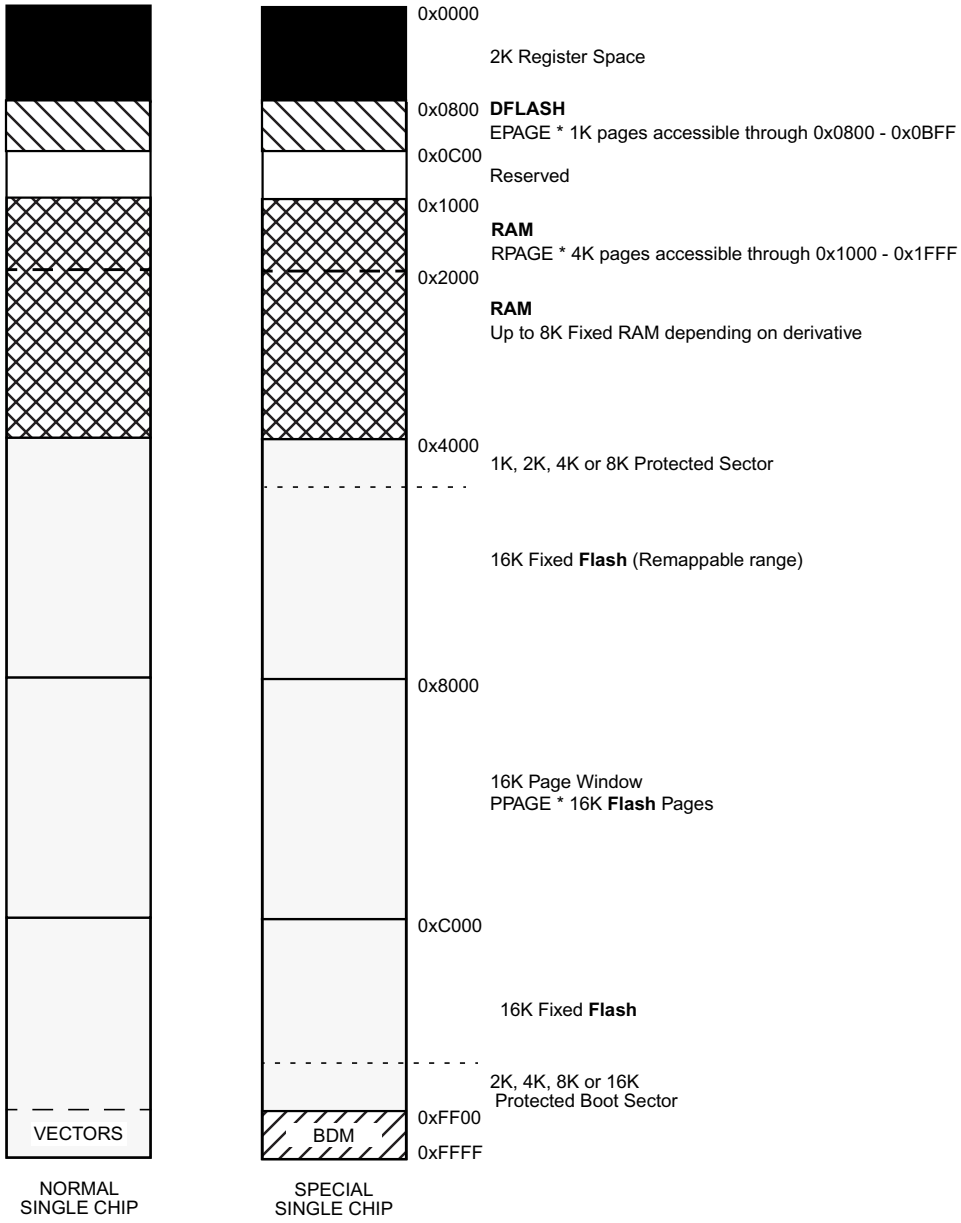

Figure 5. MC9S12XS 16-bit Memory Map

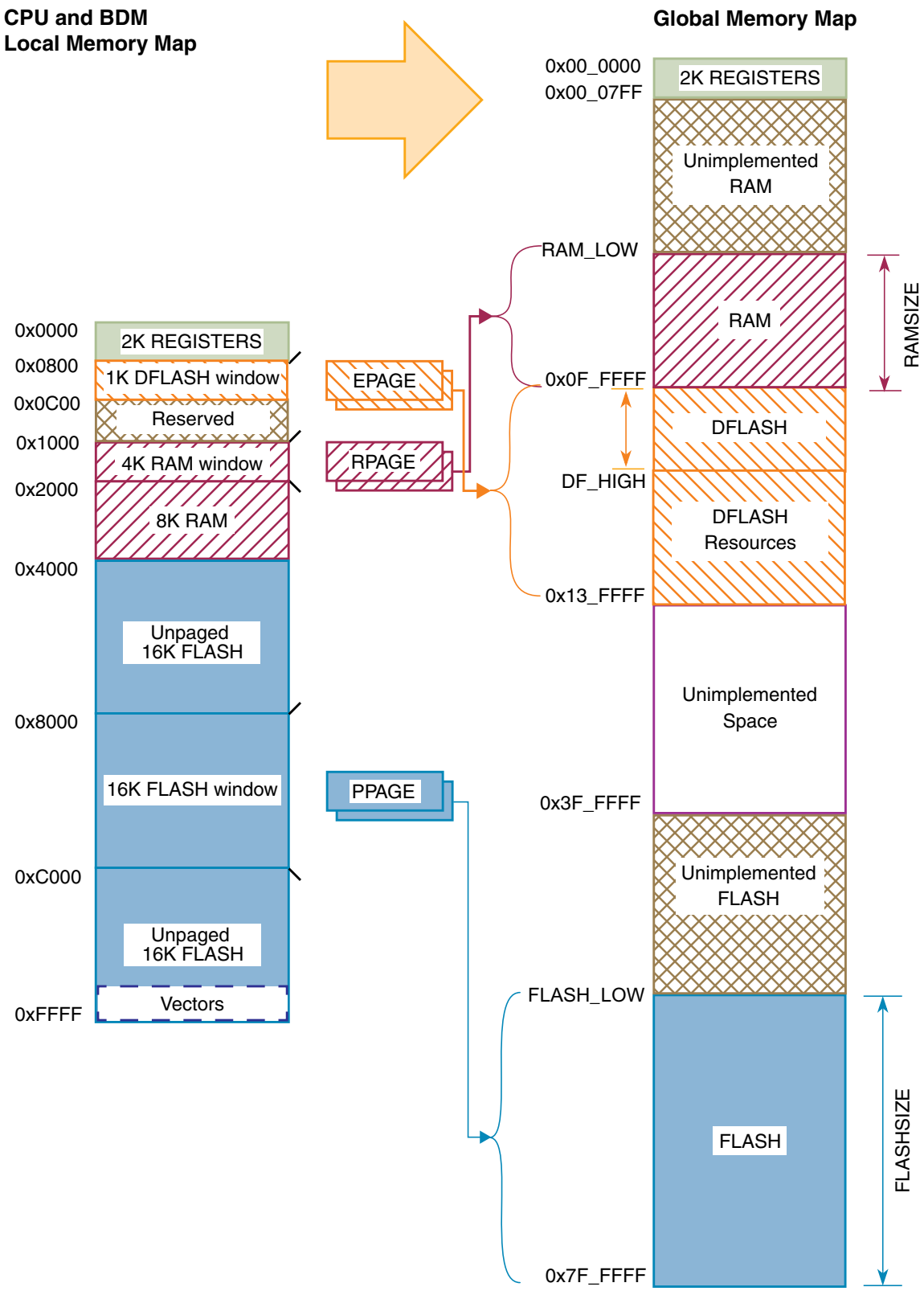

Figure 6 MC9S12XS Global Memory Map

Table 6 Memory Sizes per Derivative

Device	FLASH_LOW	SIZE/ PPAGE(1)	RAM_LOW	SIZE/ RPAGE(2)	DF_HIGH	EPAGE(3)
9S12XSx256	0x7C_0000	256K / 16	0x0F_D000	12K / 3	0x10_1FFF	8K / 8
9S12XSx128	0x7E_0000	128K / 8	0x0F_E000	8K / 2	0x10_1FFF	8K / 8
9S12XSx64	0x7F_0000	64K / 4	0x0F_F000	4K / 1	0x10_0FFF	4K / 4

NOTES:
1. Number of 16K pages addressable via PPAGE register
2. Number of 4K pages addressing the RAM.
3. Number of 1K pages addressing the DFLASH

Revision History

Table 7 Revision History

Version Number	Revision Date	Author	Description
0.00	12-Jan-2006	DB	Initial version. Based on 9S12XEFAMPP rev 0.10
0.01	27-Mar-2006	DB	Removed ECLKX2 Added 48qfn mechanical diagram Altered 48pin and 52pin pinouts - share VRH/VDDA1 & VRL/VSSA1. Changed and simplified routing of peripherals.
0.02	29-Mar-2006	DB	Fixed SPI signal ordering on Port M Fixed various typos Added VRH, VRL, VDDA and VSSA to block diagram
0.03	4-Apr-2006	RF	Removed SPI from PM[0:1,6:7] Added SCI1 to PM[0:1] Altered 48pin and 52pin pinouts
0.04	6-Apr-2006	RF	Removed routing options for SCI1, PWM, TIM on 112 and 80 Removed SPI from PP[0:3]
0.05	7-Apr-2006	RF	Added SCI1 to PT[0,2]
0.06	28-Apr-2006	DB	Updated Block Diagram to reflect peripheral routings. Added SPI0 routing to PS[7:4] in Table 4.

Table 7 Revision History

Version Number	Revision Date	Author	Description
0.07	22-Jun-2006	DB	Changed VSSR to VDD3. DFlash sector size 256 bytes. Added Global Memory map Figure 6 & Table 6. Removed 5 Fuzzy instructions.
0.08	16-Aug-2006	DB	Changed Interrupt Module to 7 levels of interrupt.
0.09	28-Nov-2006	DB	Removed 52QFP and 48LQFP package options Added 64LQFP package option Modified PortT pinout on 48QFN,
1	08-Dec-2006	DB	Minor formatting changes
2	1-Jun-2007	DB	Removed 48QFN package option Added 64qfp option for XS256 Change routing option to remove PWM0-3 from PT0-3
3	19-Jun-2007	DB	Correction to Table 2: 8PWM channels available in all packages.
4	11-Nov-2008		Removed ROM options Added KGD options Removed package drawings

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