

MPC5606E Microcontroller Product Brief

The MPC5606E microcontroller is the newer member of the Qorivva 32-bit microcontroller family built on Power Architecture(R) technology and integrates MPC5604E device with the Broadcom(R) BCM89810 single-port BroadR-Reach™ 100 Mbps automotive Ethernet transceiver. This device is targeted at the chassis and safety market segment visual-based driver assistance, especially the CMOS Vision Sensor Gateway, Radar Sensor Gateway, and Infotainment Network Gateway.

The MPC5606E microcontroller is a gateway system designed to move data from different sources via Ethernet to a receiving system and vice versa. The supported data sources and sinks are:

- Video data (with 8/10/12 bits per data word)
- Audio data (6× stereo channels)
- RADAR data (2 × 12 bit with <1μs per sample, digitized externally and read in via DSPI)
- Other serial communication interfaces including FlexCAN, LINFlex, and DSPI

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Block diagrams

The Ethernet has a bandwidth of 10/100 Mbits/sec supporting precision time stamps (IEEE1588). Unshielded twisted pair cables are then used to transfer information (via Ethernet) in the car. Thus, a significant reduction of wiring costs in the car can be achieved by providing high bandwidth data links.

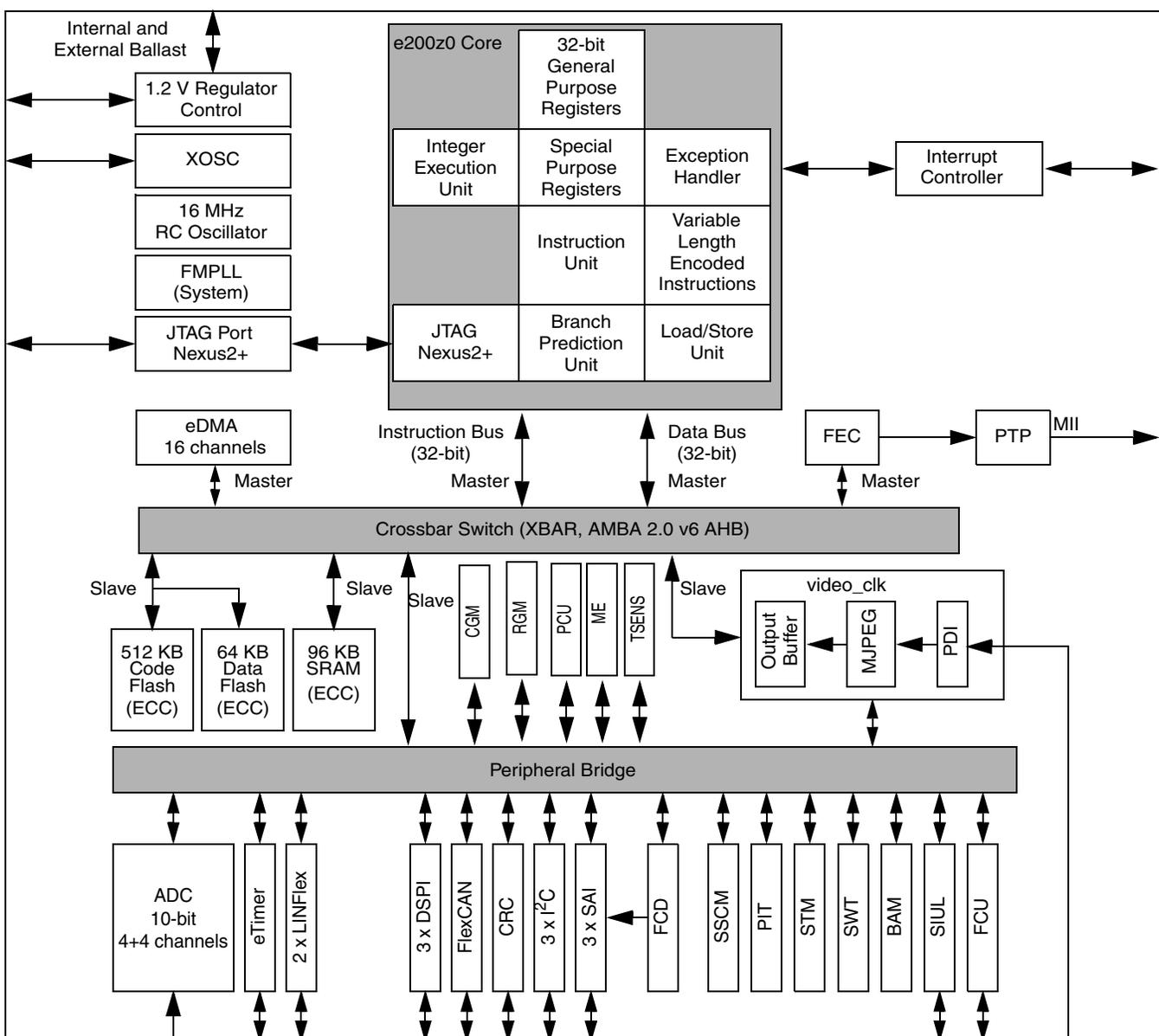
The Ethernet Audio Video Bridging (AVB) is an upcoming high-bandwidth communication standard in the automotive area competing with established protocols like LVDS, MOST, and FlexRay.

The BCM89810 is a 100 Mbps automotive Ethernet transceiver integrated into a single monolithic CMOS chip. The device performs all of the physical layer (PHY) functions for BroadR-Reach™ encoded Ethernet packets over single-pair unshielded twisted-pair copper wire, such as FlexRay™. The BCM89810 is designed to exceed automotive specifications for noise cancellation and transmission jitter, providing consistent and reliable operation over the broadest range of existing single-pair twisted-pair automotive cable plants.

1 Block diagrams

1.1 MPC5604E block diagram

Figure 1 shows a top-level block diagram of the MPC5604E device.



- | | | | |
|------------------|--|-------|--|
| ADC | Analog-to-Digital Converter | CGM | Clock Generation Module |
| BAM | Boot Assist Module | PCU | Power Control Unit |
| CRC | Cyclic Redundancy Check | RGM | Reset Generation Module |
| DSPi | Deserial Serial Peripheral Interface | TSENS | Temperature sensor |
| eDMA | Enhanced Direct Memory Access | MJPEG | 12-bit Motion JPEG Encoder |
| eTimer | Enhanced Timer | PDI | Parallel Data Interface (image sensor) |
| FCD | Fractional Clock Divider | PIT | Periodic Interrupt Timer |
| FCU | Fault Collection Unit | PTP | IEEE 1588 Precision Time Stamps |
| FEC | Fast Ethernet Controller | SIUL | System Integration Unit |
| FlexCAN | Flexible Controller Area Network | SRAM | Static Random-Access Memory |
| FMPLL | Frequency-Modulated Phase-Locked Loop | SSCM | System Status and Configuration Module |
| I ² C | Inter-Integrated Circuit serial interface | STM | System Timer Module |
| SAI | Serial Audio Interface 6xStereo | SWT | Software Watchdog Timer |
| LINFlex | Serial Communication Interface (LIN support) | | |
| ME | Mode Entry Module | | |

Figure 1. MPC5604E block diagram

Table 1. Block diagram components

Module	Domain	Functional grouping	Description
1.2 V Regulator	Analog and Digital	Power Supply	Regulates 1.2 V core (logic) power supply. Controls the internal ballast transistor.
ADC	Analog	Application	10-bit Analog to digital converter with 10 bit, 1µs/sample and 4 input channels (plus 4 internal).
BAM	Digital	Boot	Reads device settings and execute boot code including input probing.
Code Flash, Data Flash (PFlash controller)	Digital	Core System	Crossbar slave. ECC protected Code and Data Flash. The flashes are connected via a 4 × 128-bit buffer, supporting pre-fetches to reduce wait times due to the 2 wait state reads from the flash array.
CRC	Digital	Communication	Computes checksums for data streams coming via the communication interfaces.
DSPI	Digital	Communication Interfaces/Media Interfaces	SPI interface allowing to connect analog-to-digital converters, sensors, and actuators.
e200z0 Core	Digital	Core System	Cacheless e200z0 PowerPC CPU with Harvard architecture.
eDMA	Digital	Core System	16 channel direct memory access interface, enables transfer of data without CPU interaction. Peripherals, e.g., ADC, can trigger data transfers from an internal register to system SRAM and vice versa.
eTimer	Digital	Application	Timer to measure external input events or to create pulse modulated outputs.
FCD	Digital	Clock	Provides fine tuned clocks for the audio interface or the video clock.
FCU	Digital	Safety	Enables tracking of system failures (Low supply voltage, lost PLL, ECC errors, etc.).
FlexCAN	Digital	Communication Interfaces	Serial interface module allowing to connect to other off chip CAN components.
FMPLL	Analog	Clock	Takes XOSC clock output and scales up the frequency to the internal clock speed. Allows frequency modulation for better EMI behavior. The module provides the clock for the system.
I ² C	Digital	Communication Interfaces	Serial Inter-Integrated-Circuit configuration bus (e.g. for the external camera or audio DSP).
I2S/I2STDM (SAI)	Digital	Media Interfaces	Serial Audio Interface enables connections to an audio source or to an audio sink (DAC/DSP) with 6 stereo channels.
Interrupt Controller	Digital	Core System	Interrupt controller for the e200z0 CPU allowing to send service requests from on-chip peripherals and external pins to the CPU.
JTAG Port	Digital	Debug	IEEE 1149.1 (JTAG) port module
LINFlex	Digital	Communication Interfaces	This is a serial interface module allowing to connect to other off chip SCI (serial communication interface) components.
CGM	Digital	Core System	Provides logic and control required for the generation of system and peripheral clocks
PCU	Digital	Core System	Power Control Unit.

Table 1. Block diagram components (continued)

Module	Domain	Functional grouping	Description
RGM	Digital	Core System	Centralizes reset sources and manages the device reset sequence of the device
NPC	Digital	Debug	Nexus port controller. Also include device number
Peripheral Bridge	Digital	Core System	Crossbar slave translating AMBA transactions from the crossbar to IPS transactions to the system peripherals. Bridge also does the address decoding for the individual slaves on the IPS bus.
PIT	Digital	Core System	Produces periodic interrupts and triggers.
RC Oscillator	Analog	Clock	Internal 16 MHz oscillator. This oscillator is used at boot time and in failure mode.
SSCM	Digital	Core System	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable.
SIU	Digital	I/O System	Controls pad configurations for selecting different functionality mapped to pad. Also controls GPIO functionality (input, output interrupt).
SRAM (SRAM controller)	Digital	Core System	ECC protected system SRAM (Static Random Access Memory) allowing zero wait state accesses.
STM	Digital	Core System	Provides a set of timers to the CPU.
SWT	Digital	Safety	Detects SW taking wrong branches and leaving expected instruction flow.
TSens	Analog	Safety	Monitors if the MCU operates in a valid temperature range.
Video Encoder	Digital	Media Interfaces	Consists PDI (parallel data interface) for video data input, input buffer, MJPEG video encoder and output buffer.
XBAR	Digital	Core System	Crossbar to allow simultaneous access from the masters (e200z0 core, eDMA, Ethernet) to the slave devices (SRAM, Flashes, Video Out Buffer, peripherals).
XOSC	Analog	Clock	Module connecting to the external crystal oscillator.

1.2 BMC89810 block diagram

Figure 2 shows a top-level block diagram of the BMC89810 device.

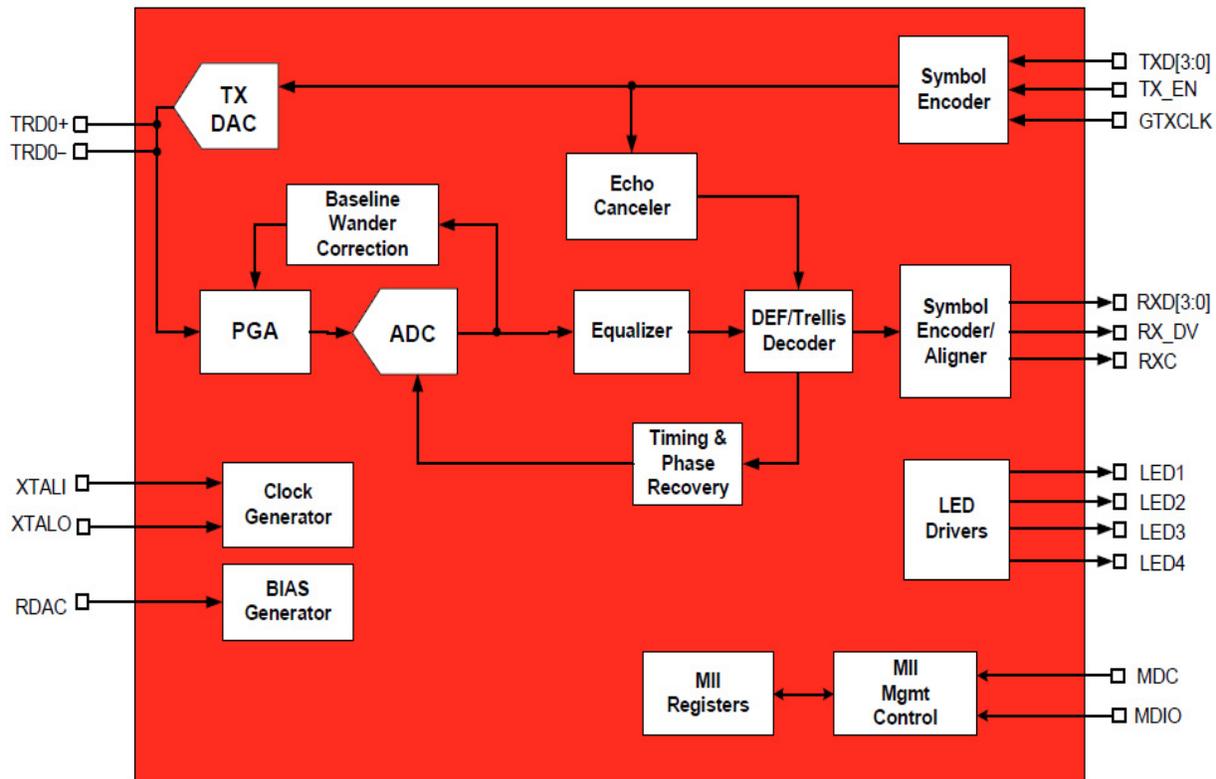


Figure 2. BMC89810 block diagram

The BCM89810 is based on Broadcom's proven digital-signal processor technology, combining digital adaptive equalizers, ADCs, phase-locked loops, line drivers, encoders, decoders, echo cancelers, and all other required support circuitry. The BCM89810 is designed to be fully compliant with RGMII and MII interface specifications, allowing compatibility with industry-standard Ethernet media access controllers (MACs) and switch controllers. The device detects and corrects polarity automatically. BroadR-Reach technology enables the BCM89810 to auto-negotiate and link up with BroadR-Reach compliant link partners. The BCM89810 delivers the most comprehensive automotive technology solution required by OEM and Tier 1 suppliers, meeting or exceeding CISPR 25 component-level, ISO 11452-5 Stripline, ISO 11452-4, IEC 61000-4-2, AEC-Q100, and Grade 1 temperature range.

2 Application examples

The following sections contain examples of applications for the MPC5606E microcontroller.

2.1 CMOS vision sensor gateway

The active safety and advanced driver assistance systems (ADAS) support Panorama View Park-Assist providing a high quality view of the vehicle's surroundings (typically a bird's eye view).

For this, up to 5 CMOS cameras with wide-angle lenses attached to the car. A typical installation has one camera at each corner of the front bumper, one in each side mirror and one in the rear. The front-viewing sensors cannot be combined with the front-viewing camera sensor used for active safety applications due to completely different optical requirements. All sensors are connected to a central fusion Electronic Control Unit (ECU) that performs enhancement and image generation.

First, the fusion unit corrects the wide-angle distortion in each image, if not done optically. Alternatively, there is an inexpensive optical solution (2nd inverting lens) on the market.

The next step is the stitching of the images—similar to the feature found on many of today’s digital cameras. There is a broad range of algorithm complexity depending on the required quality. In principle, similarities in adjacent images need to be identified, e.g., by running matching filters. After identifying how the images fit geometrically together, there is some post-processing necessary for a smooth appearance within the overlapping areas.

Finally, the stitched images are rendered on a 3D grid model representing the chosen perspective to generate the final image.

The interconnect between the remote cameras and central fusion unit is done in a point-to-point manner with a switch located in the central ECU. The switch combines the Ethernet AVB streams and sends them, e.g., via GigE, to the central processing unit. Future systems with more ADAS nodes (e.g., cameras and RADARs in the bumper) might have two dedicated ADAS switches.

Figure 3 illustrates a multi-camera system based on the MPC5606E.

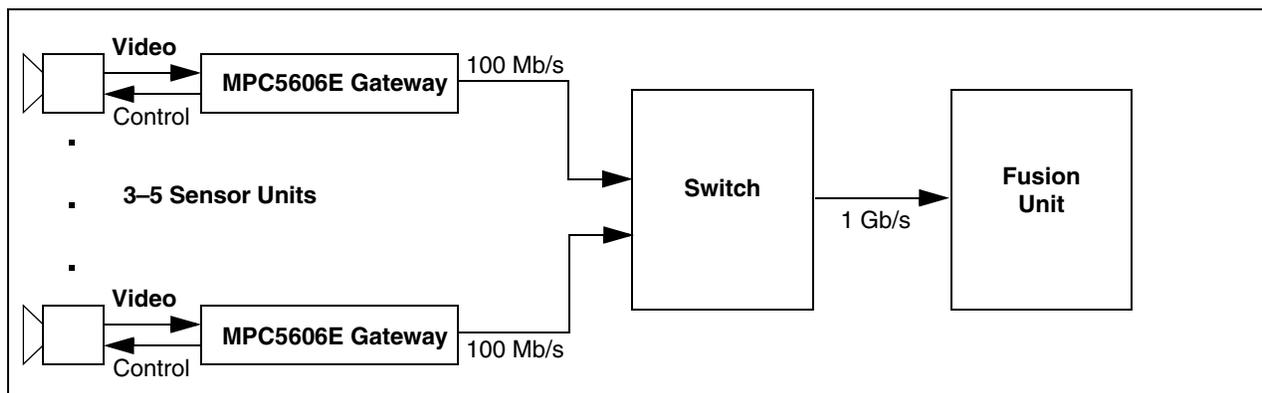


Figure 3. Multi-camera system level diagram

Each camera is connected to one MPC5606E gateway via a parallel digital interface as shown in Figure 4. The raw data is buffered and the color component is vertically sub-sampled from YUV4:2:2 to YUV4:2:0. A low latency video encoder compresses the image data by a factor of 1:5/1:10 or higher into a bit stream. This compression is not lossless, thus, the quality of the image is degraded with higher compression ratios. The video bitstream is then buffered in the MPC5606E device (dedicated video bit stream buffer) and transmitted via the Ethernet AVB link.

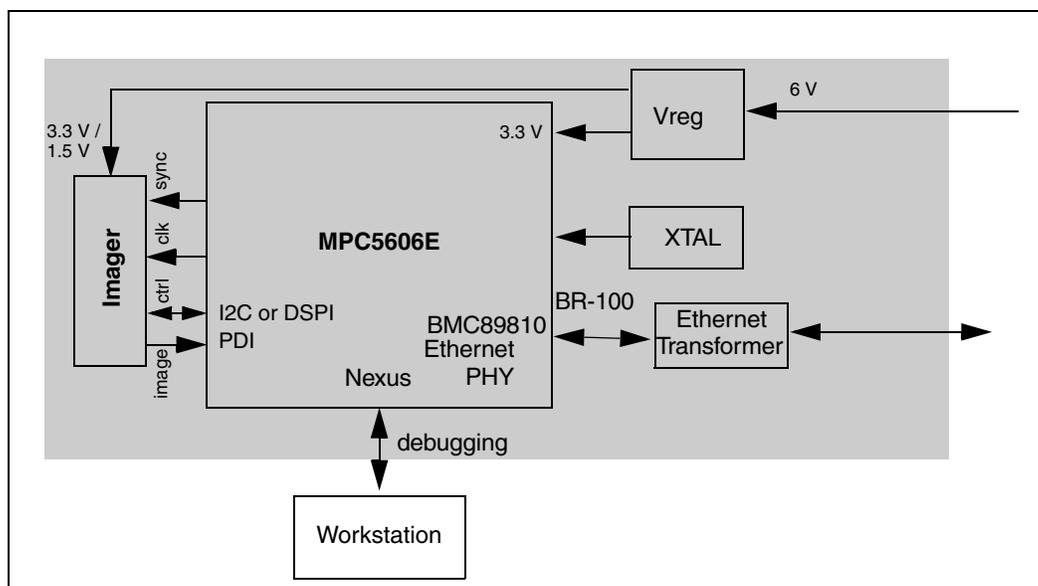
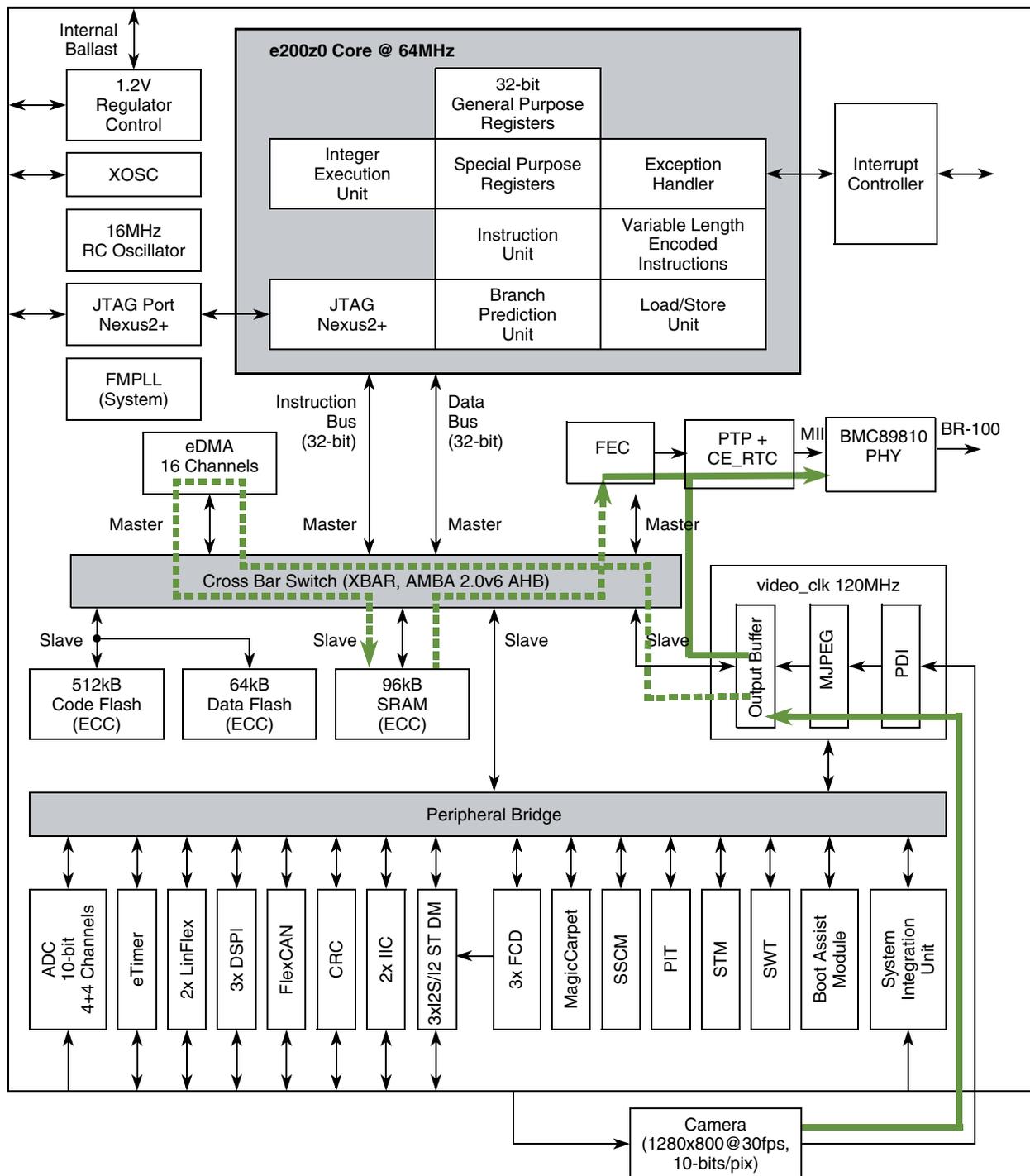


Figure 4. MPC5606E interfacing for CMOS sensor gateway

Figure 5 illustrates the processing flow of video data within the MPC5606E.

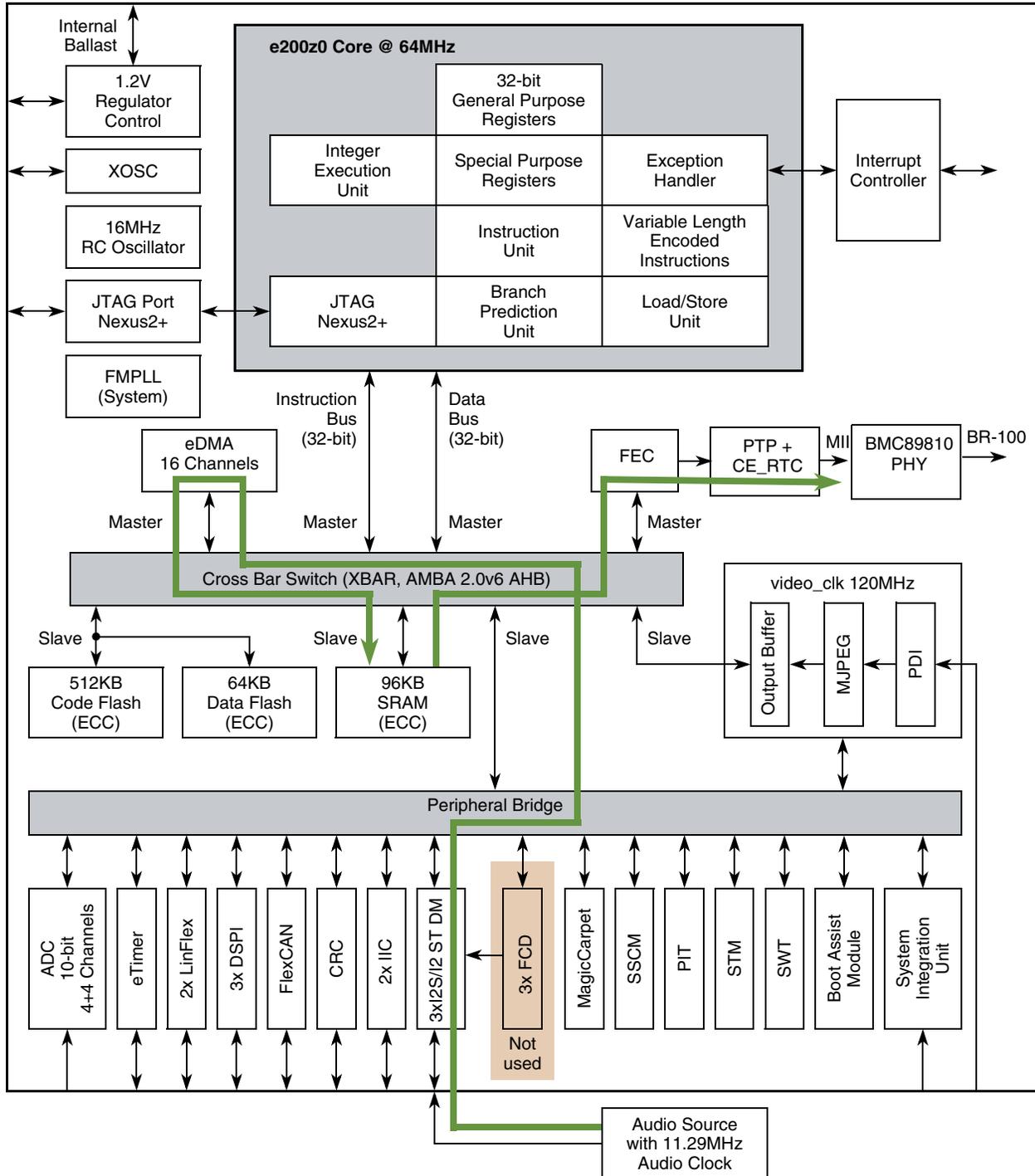


Video Encoding:
 Video data is captured by the camera, and streamed via the PDI to the Video Encoder (MJPEG). The MJPEG offers the encoded data via an output buffer memory to the FEC (Ethernet).
 Besides the video data, also histograms (for exposure control) are streamed to the PDI. The PDI separates these data that are moved via DMA to the SRAM. The CPU processes the information and set up the exposure/white balance via the IIC in the camera.

Figure 5. MPC5606E video data path

2.2 Audio source gateway

The MPC5606E can be effectively used as an audio source gateway. [Figure 6](#) shows the data flow for this application. Six stereo input audio channels at 44.1 KHz or 48 KHz are provided via I2S by an external audio source (radio, CD/DVD player, etc.). The external device provides the clock for its data (master).



Audio In:
 Data is sampled based on the input signals SAI_BCLK (11.29MHz) and SAI_SYNC. The I2S module (SAI) buffers the input data (6 channels) and signals the availability of data to the DMA module (in 64MHz domain). The DMA module moves the data to the SRAM. From here the FEC can move the data via the MII interface to a receiver.

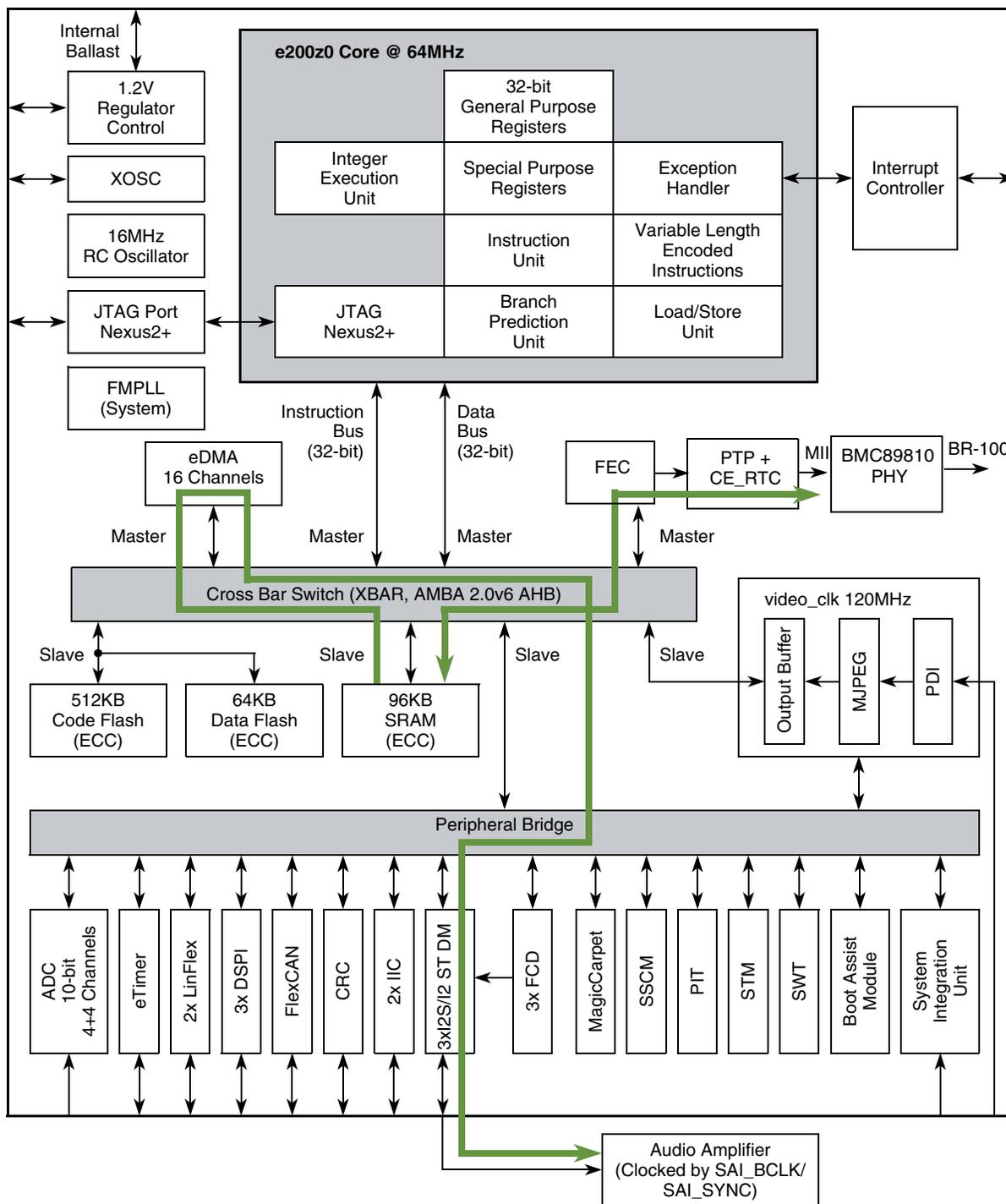
Figure 6. Audio to ethernet data path

2.3 Low cost audio output gateway

Figure 7 illustrates an audio output gateway with medium quality level. This scenario does not require an external clock generator for the audio amplifier.

The audio data (up to 6× stereo) is streamed via Ethernet port. Because the remote audio source uses its own crystal oscillator the output data rate needs to be tuned to match the stream data rate. This is done by using a fractional clock divider that results in minimum long term jitter to avoid buffer overflows and buffer underruns.

The usage of the fractional clock divider implies a certain amount of clock jitter, which is not acceptable for high end audio.

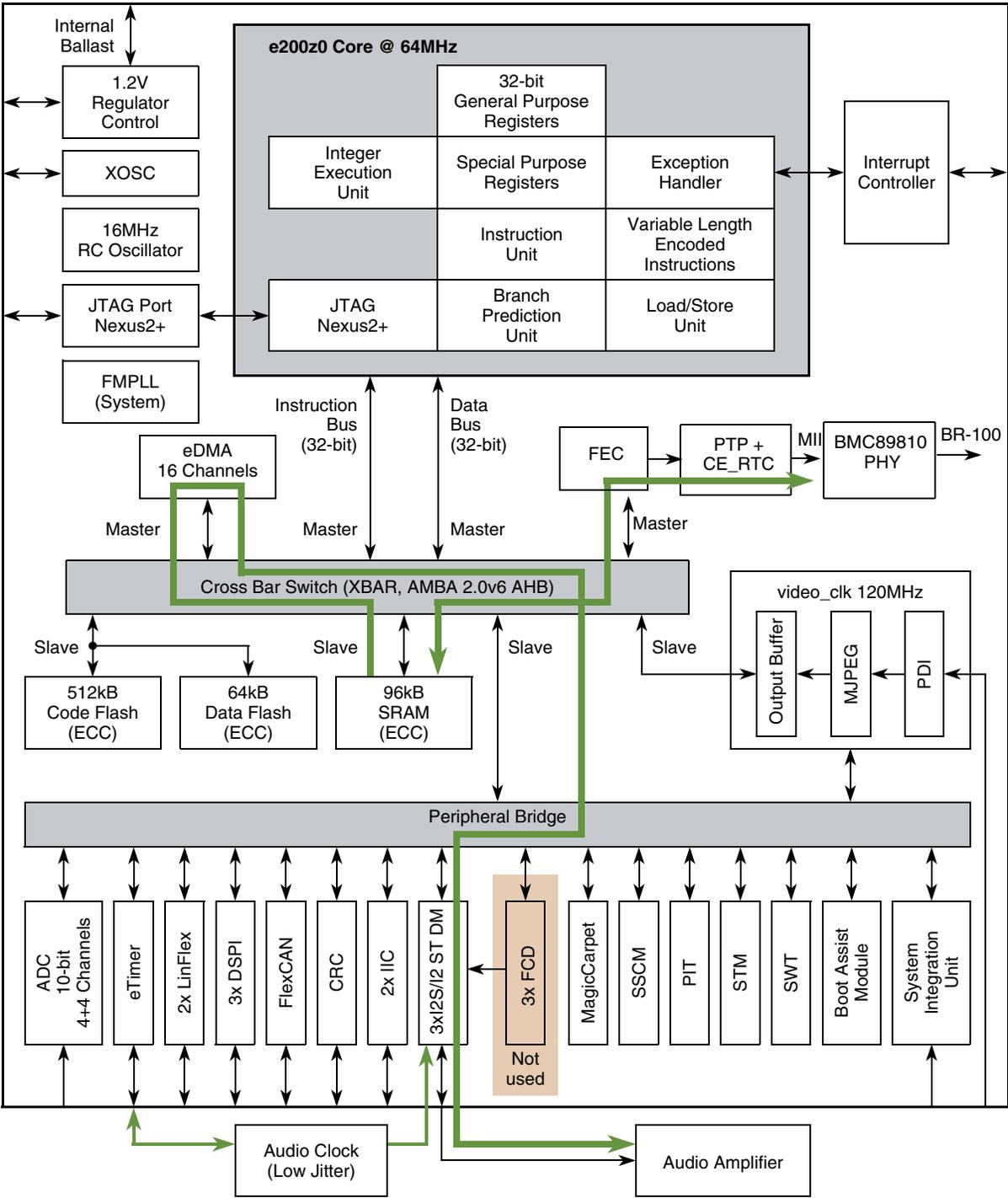


Audio Out (Low Cost):
 Data is coming via the FEC and is stored in the SRAM. From here the DMA engine moved the data to the I2S buffers. The I2S outputs the audio data based on the clock generated by the fractional clock divider (FCD), that runs on a high frequency clock (e.g. for 240MHz the clock jitter will be +2.1ns peak).

Figure 7. Ethernet to audio data path with internal audio clock

2.4 High quality audio output gateway

In the high quality audio output application shown in [Figure 8](#), the MPC5606E is receiving the audio bit stream (up to 6× stereo) via the Ethernet interface. Since the audio source clock (bit stream rate) is derived from a different crystal oscillator, the audio clock needs to be tuned to avoid buffer overflows or underruns. In this scenario, an external low jitter clock generator is tuned via a pulse width modulated (PWM) signal (alternatively via I2C). To allow a closed loop control and avoid long term jitter, the audio clock must be measured. Measuring of the external audio clock is done via an eTimer input channel.

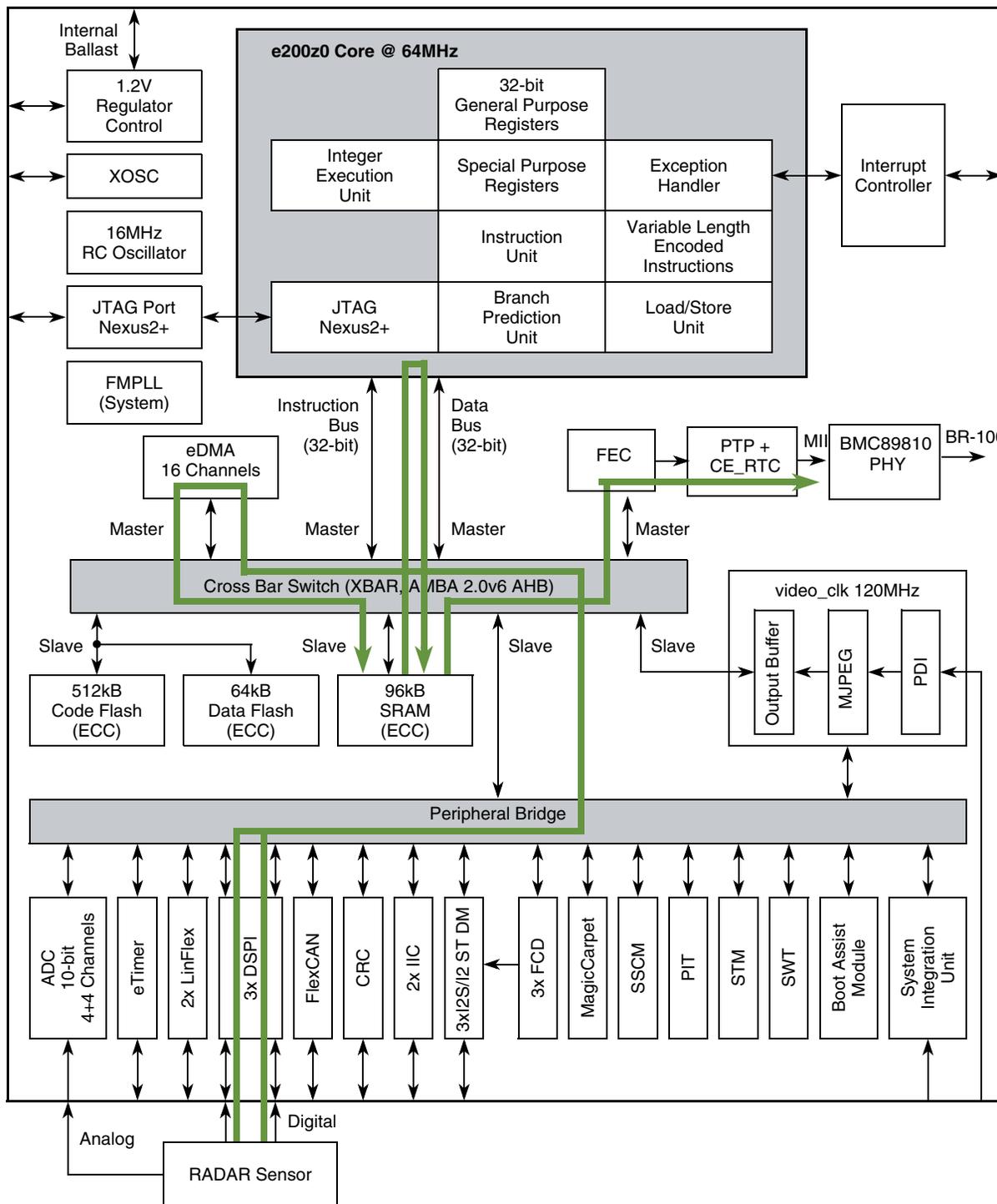


Audio Out (High Quality):
 Data is coming via the FEC and is stored in the SRAM. From here the DMA engine moved the data to the I2S buffers. The I2S outputs the audio data based on the external low jitter audio clock. To avoid buffer overflows and buffer under-runs, the external audio clock needs to be close loop controlled. For this purpose the audio clock is measured by the eTimer and adjusted using either a PWM signal from the eTimer or using the IIC module.

Figure 8. Ethernet to high quality audio data path with external audio clock

2.5 RADAR to Ethernet gateway

Figure 9 shows the processing flow for RADAR data. The RADAR data is digitized externally to the MPC5606E. The digitized samples are sent via DSPI (2 channels at 12 bits/sample \times 1MHz) to the MPC5606E. The MPC5606E performs a software implemented FFT on the RADAR data before sending out via the Ethernet.



RADAR:
 RADAR data is sampled and converted to digital by the ADC (or read via DSPI). From here the data is transported using the DMA to the SRAM. The CPU performs a FFT and writes back the data to the SRAM. Now the FEC can read out the transformed RADAR data and send them via Ethernet.

Figure 9. RADAR to Ethernet data path

NOTE

In addition to the two DSPI modules used to read the RADAR data, MPC5604E devices has a third DSPI interface used to communicate to the control part of external the RADAR components.

3 Features

The following sections give an overview of the architecture and features of the MPC5606E device.

3.1 BMC89810 architectural features

The BMC89810 architectural features are listed below.

- Single BroadR-Reach transceiver in a fully integrated 65 nm CMOS chip
- Full-duplex operation at the rate of 100 Mbps over one pair of UTP cable
- Fully integrated twisted-pair termination resistors
- Trace-matched output impedance

3.2 MPC5606E feature summary

Table 2. Device summary

Feature	MPC5606E
	121MAPBGA
CPU	e200z0h, 64 MHz, VLE only, no SPE
Flash with ECC	CFlash: 512 KB (LC) DFlash: 64 KB (LC, area optimized)
RAM with ECC	96 KB
DMA	16 channels
PIT	yes
SWT	yes
FCU	yes
Ethernet	100 Mbits MII-Lite
Video Encoder	8bpp/12bpp
Audio Interface	6x Stereo (4x synchronous + 2x synchronous/asynchronous)
ADC (10-bit)	1× 4 channels + V _{DD_IO} + V _{DDCore} + TSens
Timer I/O (eTimer)	1×6 channels
SCI (LINFlex)	2×
SPI (DSPI)	DSPI_0: 2 chip selects DSPI_1: 2 chip selects DSPI_2: 4 chip selects
CAN (FlexCAN)	1×

Table 2. Device summary (continued)

Feature	MPC5606E
	121MAPBGA
IIC	2×
Supply	3.3 V IO 1.2V Core with dedicated ballast source pin in two modes: <ul style="list-style-type: none"> • internal ballast or • external supply (using power on reset pin)
Phase Lock Loop (PLL)	1× FMPLL
Internal RC Oscillator	16 MHz
External crystal Oscillator	4 MHz - 40 MHz
CRC	yes
Debug	JTAG
Ambient Temperature	-40 to 125 °C

3.3 Critical performance parameters

MPC5606E is running under the following critical performance corner points:

- Maximum CPU frequency: 64 MHz
- Junction temperature range: -40 °C to 125 °C¹
- Nominal power dissipation: Less than 1.5 W
- Supply voltages:
 - $V_{DD_HV_IO} = 3.3V$
 - $V_{DD_HV_ADC} = 3.3V$
 - $V_{DD_HV_Core} = 1.2V$ (with internal ballast or external supply)

3.4 Module feature list

3.4.1 High performance e200z0 core CPU

The e200z0 Power Architecture core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU
- Harvard architecture

¹ Ambient temperature is 125 °C, for the video use case with internal core voltage supply the ambient temperature is 105 °C.

Features

- Variable length encoding (VLE), allowing mixed 16-bit and 32-bit instructions
- Results in smaller code size footprint
- Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
- 1-cycle load latency
- Misaligned access support
- No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non Maskable Interrupt support

3.4.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for concurrent transactions to occur from any master port to any slave port. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. The default priority scheme is fixed priority based on the master ID. Besides this, the software can select a round robin arbitration.

The crossbar provides the following features:

- Four master ports
 - e200z0 core complex Instruction port
 - e200z0 core complex Load/Store Data port
 - eDMA
 - Ethernet
- Four slave ports
 - Flash memory (code flash and data flash) controller
 - SRAM controller
 - Video encoder output buffer
 - Peripheral bridge
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on port master

- Temporary dynamic priority elevation of masters

3.4.3 System clocks and clock generation

The following list summarizes the system clock and clock generation on the MPC5606E:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider ($\div 1$, $\div 2$, $\div 4$, $\div 8$)
- Fractional clock divider clock for close loop controlled clocks
 - Provides audio clock in medium quality mode (approximately 11.29 MHz)
 - Provides camera input clock (25–30 MHz)
- On-chip oscillator with automatic level control
- Internal 16 MHz RC oscillator for rapid start-up and safe mode
 - Supports frequency trimming by user application
- Ethernet TX clock as input for the PLL (via OSC input pin)
- Up to 64 MHz for system clock; up to 128 MHz for video encoder clock

3.4.4 Frequency Modulated Phase Lock Loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to re-lock
- Frequency modulated PLL
- Modulation enabled/disabled through software
- Triangle wave modulation
- Programmable modulation depth ($\pm 0.25\%$ to $\pm 2\%$ deviation from center frequency)
- Programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

3.4.5 Main oscillator

The main oscillator provides these features:

- Input frequency range 4 MHz to 40 MHz
- Crystal input mode or Oscillator input mode
- PLL reference

3.4.6 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC Oscillator provides these features:

- Nominal frequency 16 MHz
- $\pm 5\%$ variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

3.4.7 Voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Available in two modes
 - Using internal PMOS ballast transistor to regulate external 3.3 V down to 1.2 V for the core logic
 - Disabled for using external supply for core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

3.4.8 System Integration Unit (SIU-Lite)

The MPC5606E SIU-Lite controls MCU pad configuration, external interrupt, general purpose I/O (GPIO), and internal peripheral multiplexing.

The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIU provides the following features:

- Centralized general purpose input output (GPIO) control
 - 71 GPIO pads (bonding to pins is package dependent)
- As many as four internal output functions can be multiplexed onto one pin
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins can be alternatively configured as both general purpose input or output pins
- Direct readback of the pin value is supported on all pins through the SIU supporting 4 external interrupts based on general purpose input pins
- Supports 4 external interrupts based on general purpose input pins (8 pads per interrupt)
- Configurable digital input filter that can be applied to general purpose input pins with interrupt functions for noise elimination

3.4.9 Boot Assist Module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all MPC56XX devices that are based on the e200z0h core. The BAM program is executed every time the device is powered-on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Boot from Internal Code Flash
 - Selected as default (using internal pull down on FAB pin).
 - Censorship mode to protect the content of the flash memory.
- Alternate serial boot-loading via FlexCAN, LINFlex
 - BAM accepts a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory.

3.4.10 Junction temperature sensor

The MPC5606E has a junction temperature sensor to enable measurement of the temperature of the silicon via the ADC.

The junction temperature sensor has these key parameters:

- Nominal temperature range from $-40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$
- Calibrated sensor accuracy:
 - $\pm 10\text{ }^{\circ}\text{C}$, -40 to $25\text{ }^{\circ}\text{C}$ ambient
 - $\pm 7\text{ }^{\circ}\text{C}$, 25 to $125\text{ }^{\circ}\text{C}$ ambient

3.4.11 JTAG controller (JTAGC)

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with four pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
 - BYPASS
 - IDCODE
 - EXTEST
 - SAMPLE
 - SAMPLE/PRELOAD
- A 5-bit instruction register that supports the additional following public instructions:
 - ACCESS_AUX_TAP_NPC
 - ACCESS_AUX_TAP_ONCE

Features

- Three test data registers: a bypass register, a boundary scan register, and a device identification register.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

3.4.12 Nexus Debug Interface (NDI)

The NDI (Nexus Debug Interface) block provides real-time development support capabilities for the device Power Architecture based MCU in compliance with the IEEEISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Class 2+ standard. The development support provided includes access to the MCUs internal memory map and access to the processors internal registers during run time.

The Nexus Interface provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus 2+ features supported
- Static debug
- Watchpoint messaging
- Ownership trace messaging
- Program trace messaging
- Real time read/write of any internally memory mapped resources through JTAG pins
- Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information
- Watchpoint triggering for program tracing
- Auxiliary Output Port
- Four MDO (Message Data Out) pins in full port mode
- MCKO (Message Clock Out) pin
- Two MSEO (Message Start/End Out) pins
- EVTO (Event Out) pin
- Auxiliary Input Port
- EVTI (Event In) pin

3.4.13 DMA controller

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based

memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels support independent 8-, 16-, or 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPs, ADC, eTimer, audio interface, and video bit stream output buffer
- Programmable DMA channel mux allows assignment of any DMA source to any available DMA channel with as many as 30 potential request sources.
- eDMA abort operation through software

3.4.14 DMA channel multiplexer (DMA_MUX)

- 32 independently selectable DMA channel routers
- Each channel router is assigned to one of the following sources:
 - One of the peripheral DMA sources
 - The always enabled source

3.4.15 Software Watchdog Timer (SWT)

The SWT on the MPC5606E is configured as the SWT found on MPC5604P devices. This includes, e.g., the reset values for the timer clock selection.

The SWT has the following features:

- 32-bit time-out register to set the time-out period
- Timer running on IRC clock for increased functional safety
- Programmable selection of window mode or regular servicing
- Programmable selection of reset or interrupt on an initial time-out
- Master access protection
- Hard and soft configuration lock bits
- Reset configuration inputs allow timer to be enabled out of reset

3.4.16 System Timer Module (STM)

The STM module implements these features:

- 32-bit up counter with 8-bit pre-scaler

Features

- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

3.4.17 Periodic Interrupt Timers (PIT)

The PIT module implements these features:

- As many as four general purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel can be used as trigger for a DMA request

3.4.18 FlexCAN module

The MPC5606E MCU contains one controller area network (FlexCAN) module. This module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

- Supports the full implementation of the CAN Specification Version 2.0, Part B
 - Standard data and remote frames (up to 109 bits long)
 - Extended data and remote frames (up to 127 bits long)
 - 0 to 8 bytes data length
 - Programmable bit rate up to 1 Mbit/s
 - Content-related addressing
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as RX or TX, all supporting standard and extended messages
- Listen-only mode capability
- Individual mask registers for each message buffer
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Timestamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Programmable loop-back mode supporting self-test operation
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Wake-up when activity on the RX pin

- Requires an external glitch filter at the pad (2750 ns of 0-input)
- Wake-up via CAN interrupt
- Transmit features
 - Supports configuration of multiple mailboxes to form message queues of scalable depth
 - Arbitration scheme according to message ID or message buffer number
 - Internal arbitration to guarantee no inner or outer priority inversion
- Receive features
 - Individual programmable filters for each mailbox
 - Eight mailboxes configurable as a six-entry receive FIFO
 - Eight programmable acceptance filters for receive FIFO
- Programmable clock source
 - System clock
 - Direct oscillator clock to avoid PLL jitter

3.4.19 Deserial Serial Peripheral Interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the MPC5606E MCU and external devices (e.g., sensors).

The DSPI modules provide these features:

- Full duplex, three-wire synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- As many as four chip select lines available per DSPI module, depending on package and pin multiplexing, enable 12 external devices to be selected using external multiplexing from a single DSPI
- Eight clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering as many as five transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- TX and RX FIFOs can be disabled individually for low-latency updates to SPI queues
- Visibility into TX and RX FIFOs for ease of debugging
- Programmable transfer attributes on a per-frame basis
- Modified SPI transfer formats for communication with slower peripheral devices

3.4.20 Serial communication interface module (LINFlex)

The LINFlex on the MPC5606E features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 Specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
 - Autonomous LIN frame handling
 - LIN0 supports master and slave mode with 16 identifier filters
 - LIN1 supports master mode only (no identifier filters required)
 - Message buffer to store Identifier and as much as 8 data bytes
 - Supports message length as long as 64 bytes
 - Detection and flagging of LIN errors: Sync field; Delimiter; ID parity; Bit; Framing; Checksum and Time-out errors
 - Classic or extended checksum calculation
 - Configurable Break duration as long as 36-bit times
 - Programmable Baud rate pre-scalers (13-bit mantissa, 4-bit fractional)
 - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
 - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
 - Autonomous LIN header handling
 - Autonomous LIN response handling
- UART mode
 - Full-duplex operation
 - Standard non return-to-zero (NRZ) mark/space format
 - Data buffers with 4-byte receive, 4-byte transmit
 - Configurable word length (8-bit or 9-bit words)
 - Error detection and flagging
 - Parity, Noise and Framing errors
 - Interrupt-driven operation with four interrupt sources
 - Separate transmitter and receiver CPU interrupt sources
 - 16-bit programmable baud-rate modulus counter and 16-bit fractional
 - Two receiver wake-up methods

3.4.21 eTimer

The eTimer module provides six 16-bit general purpose up/down timer/counter.

The following features are implemented:

- Individual channel capability
 - Input capture trigger
 - Output compare
 - Double buffer (to capture rising edge and falling edge)
 - Separate pre-scaler for each counter
 - Selectable clock source
 - 0% to 100% pulse measurement
 - Rotation direction flag (Quad decoder mode)
- Maximum count rate
- Counters are cascadeable
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Counters are pre-loadable

3.4.22 Successive approximation Analog-to-Digital Converter (ADC)

The ADC module provides the following features:

- Analog part:
 - One on-chip AD converter
 - 10-bit AD resolution
 - Conversion time, including sampling time, less than 1 μ s (at full precision)
 - Typical sampling time is 150 ns min. (at full precision)
 - Differential non-linearity error (DNL) ± 1 LSB
 - Integral non-linearity error (INL) ± 1.5 LSB
 - TUE < 3 LSB
 - Single-ended input signal range from 0 to $V_{DD_HV_ADC}$
 - The ADC supply can be equal to $V_{DD_HV_IO}$ ($V_{DD_HV_ADC} = 3.3$ V)
 - The ADC supply and the ADC reference are not independent from each other (they are internally bonded to the same pad)
 - Sample times of 2 (default), 8, 64, or 128 ADC clock cycles
- Digital part:
 - 8 input channels
 - 4 channels routed to the pins
 - 4 internal connections: 1 \times temperature sensor, 1 \times core voltage, 1 \times IO voltage
 - Four analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location,

Features

- Register-based interface with the CPU: control register, status register, and one result register per channel
- ADC state machine managing 3 request flows: regular command, hardware injected command through eTimer and software injected command
- DMA compatible interface

3.4.23 Fault Collection Unit (FCU)

The FCU provides an independent fault reporting mechanism even when the CPU is not performing properly.

The FCU module includes following features:

- Collection of critical faults (all of these must be glitch free)
- Reporting of selected critical faults to external
- Fault flag status kept over non-destructive reset for later analysis (in a "Freeze" register)
- Continuous and synchronous latch of MC state
- MC state kept over non-destructive reset for later analysis (in a "Freeze" register)
- 4 states finite state machine (Init, Normal, Alarm, Fault)
- Different actions can be taken depending on fault type.
- Selectable protocols for fault signal indication in Fault state (dual-rail, time-switching, bi-stable)
- Programmable clock prescaler for time-switching output signal generation
- Protection mechanism to avoid un-wanted clearing of fault flags
- Internal logic testing, by using a fake fault generator during initialization phase

3.4.24 Cyclic Redundancy Check (CRC)

The CRC has the following major features:

- 2 contexts (static parameter) for the concurrent CRC computation
- Separate CRC engine for each context
- 0-wait states during the CRC computation (pipeline scheme)
- 3 hardwired polynomials (CRC-8, CRC-16-CCITT, CRC-32)
- Support for byte/half-word/word width of the input data stream

3.4.25 Video encoder

- Image resolution up to 1280×800 at 30 fps
- Low latency compression with MJPEG format
- Color sub-sampling from YUV4:2:2 to YUV4:2:0
- 8 bits per pixel component
- 12 bits per pixel component
- Support compression ratio from 1:20 to 1:5

- Support for the Ethernet Controller DMA via CPU Interrupt

3.4.26 Serial Audio Interface (SAI)

- Supports up to 6 (stereo) audio channels
- Transmitter with independent Bit Clock and Frame Sync supporting 4 data channels
- Receiver with independent Bit Clock and Frame Sync supporting 4 data channels
- Maximum Frame Size of 16 Words
- Word size of between 8-bits and 32-bits Word size configured separately for first word and remaining words in frame
- Asynchronous 8 × 32-bit FIFO for each Transmit and Receive Channel
- Restarts after FIFO Error

3.4.27 Ethernet AVB (FEC + PTP + RTC)

The Ethernet modules provide 100 MBits/s data communication for all use cases. To support Ethernet AVB (Audio Video Bridging), this module group consists of following modules:

- FEC (Ethernet base module)
- PTP (IEEE 1588 precision time protocol)
- RTC (Real time clock required for precision time protocol)

MPC5606E does not integrate the PHY components of the Ethernet, thus, the FEC connects via the MII-Lite interface (14 pins) to the external PHY. In addition to the MII-Lite interface, the RTC provides a single timer pin that is directly linked to the precision time.

Support for different Ethernet MAC-PHY interfaces:

- 100 Mbits/s IEEE 802.3 MII-Lite 1
- 10 Mbits/s IEEE 802.3 MII-Lite
- IEEE 802.3 full duplex flow control and half duplex flow
- Programmable max frame length
- Address recognition
- Word size configured separately for first word and remaining words in frame
- Asynchronous 4 x 32-bit FIFO for each Transmit and Receive Channel
- Graceful restart after FIFO Error:
 - Frames with broadcast address may be always accepted or always rejected
 - Exact match for single 48-bit individual (unicast) address
 - Asynchronous 4 x 32-bit FIFO for each Transmit and Receive Channel
 - Hash (64-bit hash) check of individual (unicast) address
 - Hash (64-bit hash) check of group (multicast) address
 - Promiscuous mode
- Internal loop-back

3.4.27.1 Precision Time Protocol

Hardware assistance for IEEE1588 Precision Time Protocol v1.0

- Supports user configured values for PTP header fields
- Support timestamp overrun report for TX and RX
- Supports interrupts notification due to following: RX PTP frame detection, TX
- PTP frame transmission which was marked by the Software as a PTP frame, RX and TX timestamp overrun error

3.4.27.2 RTC

Support single IEEE1588 RTC

- Support timer frequency compensation
- Support timer offset update
- One 64-bit FIPER start register. Used to define the starting time of PPS signals generation
- Support timer frequency compensation
- Separate maskable timer interrupt event register
- Phase aligned adjustable (divide by N) clock output

4 Developer environment

4.1 Software tools summary

The MPC5606E supports tools and third-party developers similar to those used for the Freescale MPC5500 product family, offering a widespread, established network of tools and software vendors. It also features a high-performance Nexus debug interface.

The following development support is available:

- Automotive Evaluation Boards (EVB) featuring CAN, LIN interfaces and more
- Compilers
- Debuggers
- JTAG and Nexus interfaces
- Autocode generation tools
- Initialization tools

The following software support is available:

- Core self tests
- Flash programming drivers
- Ethernet support

4.2 Application summary

The following list of Application software blocks are provided for the MPC5606E:

Tool	Description
Drivers	Drivers for EEPROM emulation, Ethernet stack and Video Encoder
Boot code	Boot ROM for alternate boot via LinFlex or FlexCAN module
Boot device setup	Boot code to check system errors, set up clock, Flash wait states, interrupt service routines, watchdog timer, IO configuration, and to initialize the SRAM ECC

5 Package Information

The MPC5606E is available in 121pin, 8x8 mm, low profile, Molded Array Process Ball Grid Array (MAPBGA) package.

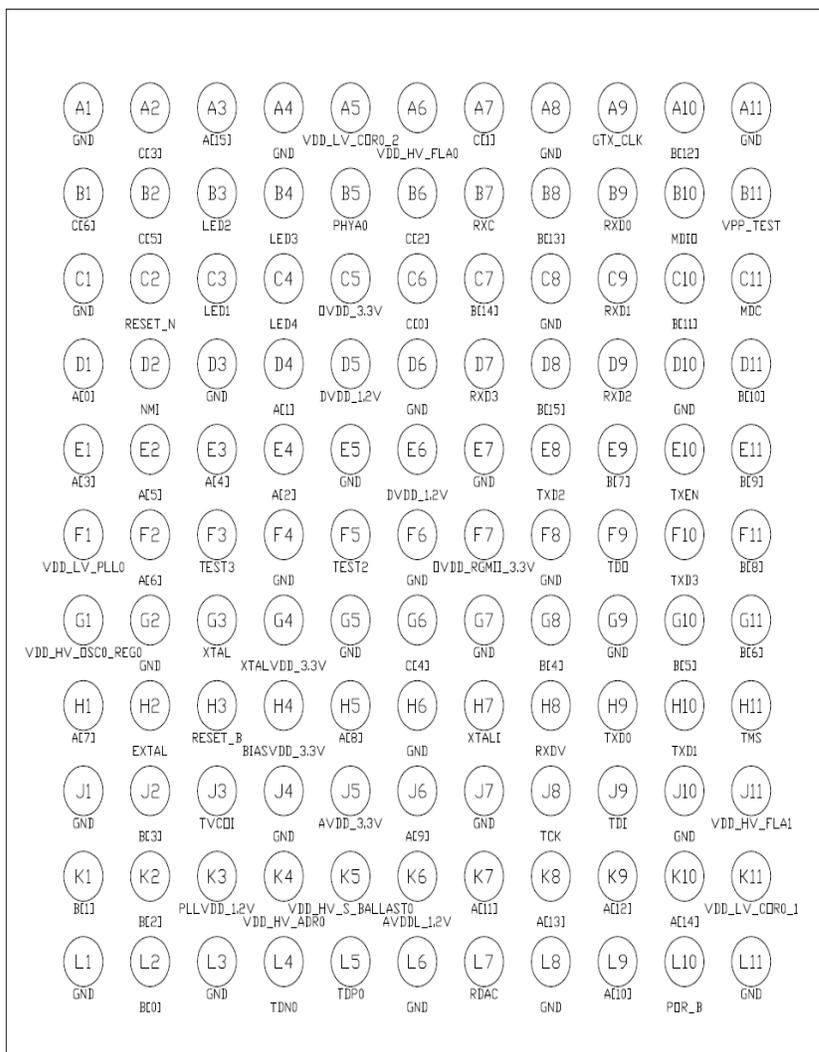
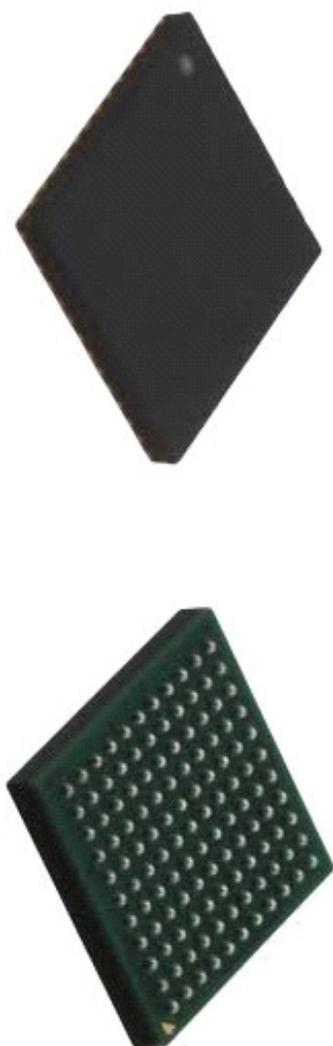


Figure 10. MPC5606E ball map

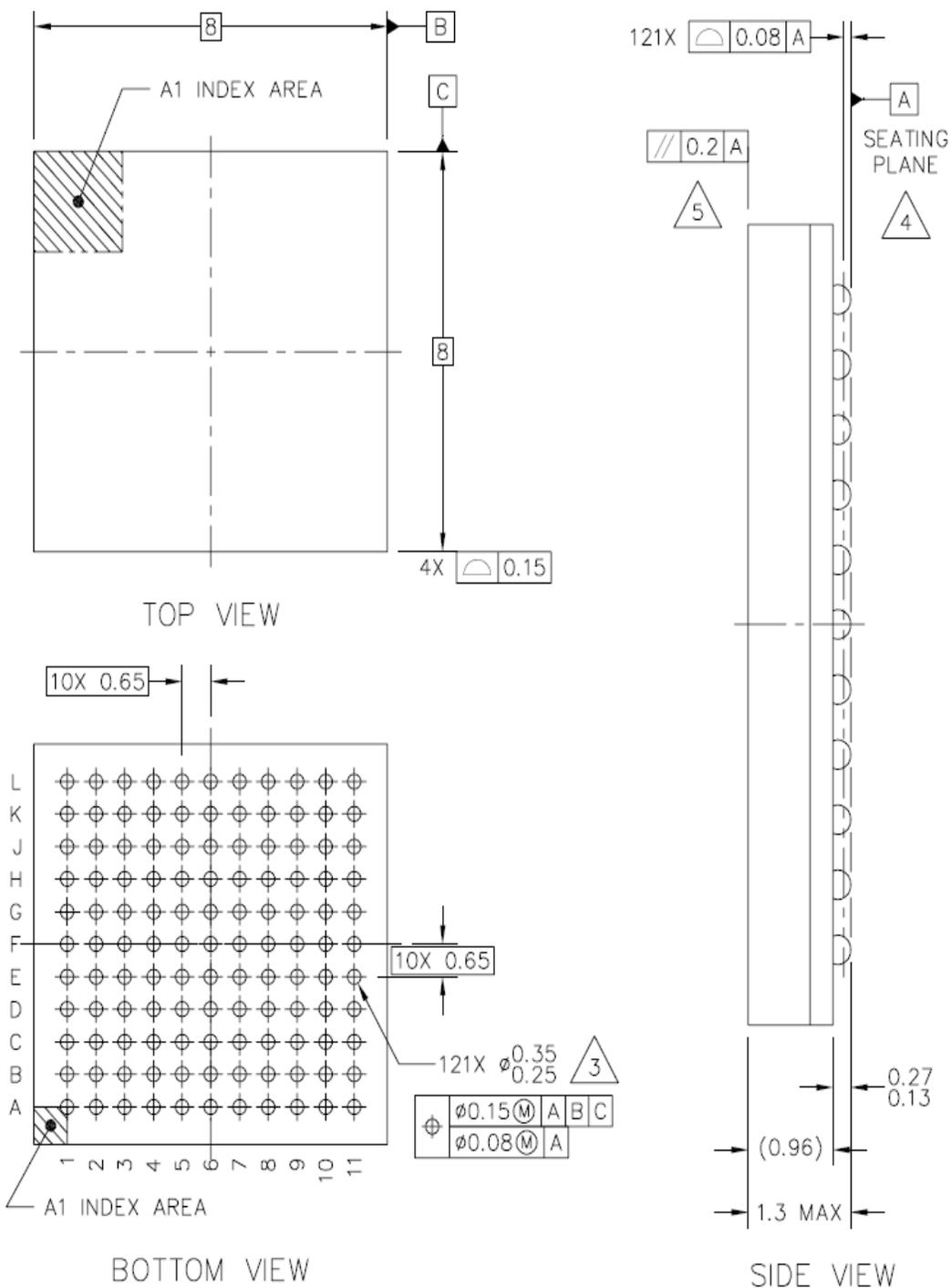


Figure 11. PBGALow Profile Fine Pitch 121 I/O 8x8 PKG, 0.65mm Pitch (Map)

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