PB_GD3160

Advanced gate driver for SiC MOSFETs and IGBTs

Rev. 2 — 17 March 2023 Product brief

1 About this document

This document is intended to provide overview/summary information for the purpose of evaluating a product for design suitability. It is intended for quick reference only and should not be relied upon to contain detailed and full information.

2 General description

The GD3160 is an advanced single-channel gate driver designed to drive the latest SiC and IGBT modules for xEV traction inverters, OBC and DC-DC converters.

GD3160 offers integrated galvanic isolation, a programmable interface via SPI, and advanced programmable protection features, such as overtemperature, desaturation, and current sense protection. GD3160 capably drives SiC MOSFETs and IGBT gates directly: its high gate current and programmable gate drive voltage features provide high performance switching, low dynamic on-resistance, and rail-to-rail gate voltage control.

The GD3160 autonomously manages faults and reports power device and gate driver status via the INTA and INTB pins, and the SPI interface. GD3160 includes self-test, control and protection functions for design of high reliability systems (ASIL C/D) and meets the stringent requirements of automotive applications, being fully AEC-Q100 grade 1 qualified.

3 Simplified application diagram

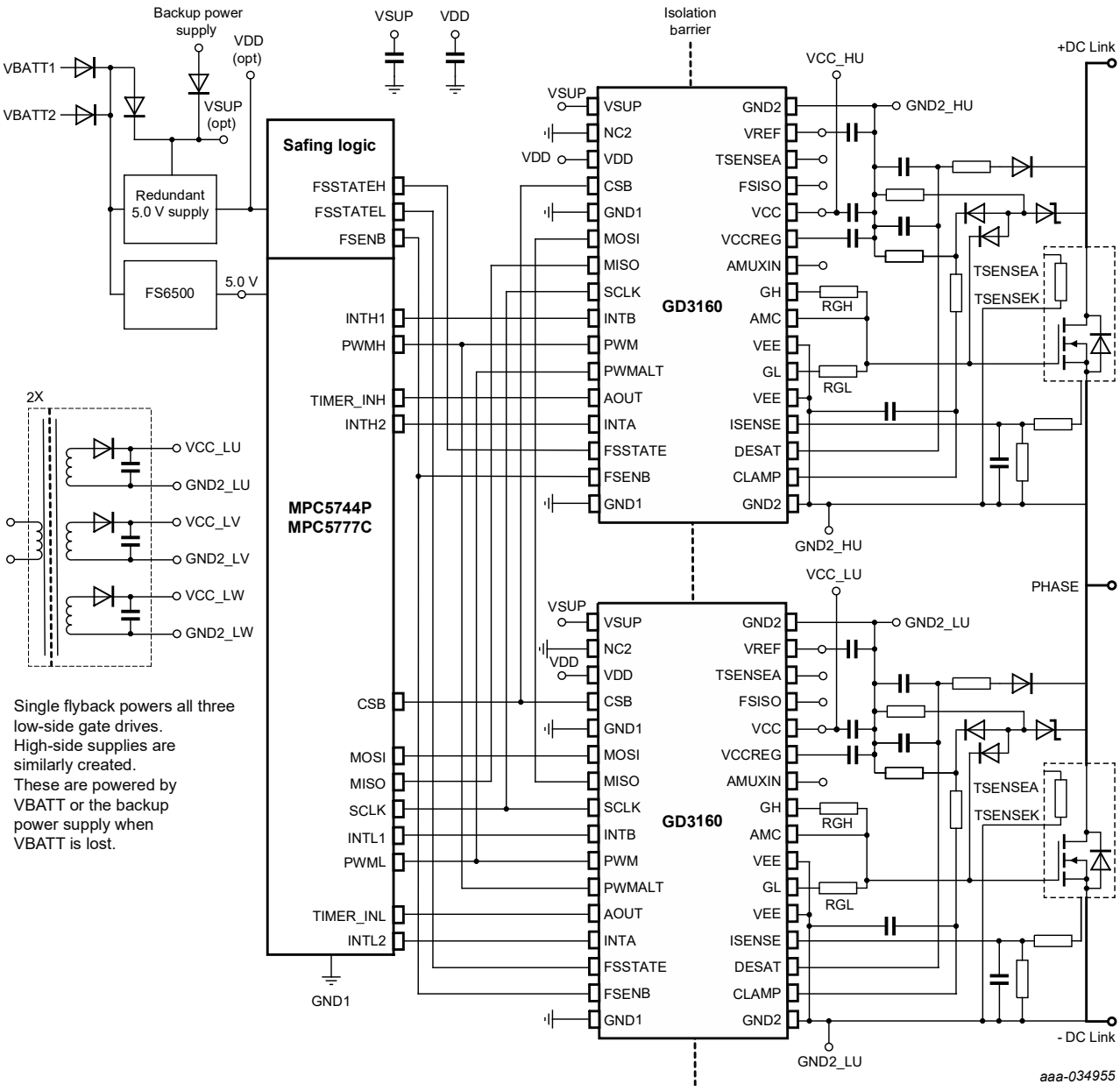


Figure 1. Simplified application diagram

4 Features and benefits

This section summarizes the key features, safety features, and regulatory approvals for the GD3160.

4.1 Key features

- Integrated Galvanic signal isolation (up to 8 kV)
- High gate current integrated: 15 A source/sink capable
- SPI interface for safety monitoring, configuration, and diagnostic reporting
- Supports high switching frequencies: PWM up to 100 kHz
- Fail-safe state management from LV and HV domain for user-selectable safe state
- Programmable gate voltage regulator over an expanded range
- Temperature sense compatible with NTC and PTC thermistors
- Configurable desaturation and current sense optimized for protecting SiC and IGBTs
- Integrated soft shutdown, two-level turn-off, optimized for unique gate drive requirements of SiC
- Real-time VCE and VGE monitoring via INTA pin
- Integrated ADC for monitoring parameters from HV domain
- CMTI > 100 V/ns
- Compatible with 200 V to 1700 V IGBT/SiC, power range > 125 kW
- Operating temperature range −40 °C to 125 °C
- External Creepage distance (CPG): > 7.8 mm
- Available in 3.3 V or 5.0 V I/O logic interface variants
- Small package footprint (8 mm x 13 mm) 32-pin SOIC

4.2 Safety features

- ISO 26262 ASIL D certified supporting ASIL D system level functional safety
- Error checking of SPI and configuration data with 8-bit CRC
- Autonomously manages severe faults and reports status via configurable INTB and/or INTA pins, and SPI interface
- Ultra-fast current, DESAT, and temperature sense inputs and ADC reporting for IGBT/SiC monitoring and protection
- Interrupt pins (INTA and INTB) for fast response to faults
- Built-in self-check of all analog and digital circuits
- Continuous watchdog of communications across isolation barrier
- Deadtime enforcement
- Over and undervoltage supervision of all power supplies on both low and high voltage sides
- Dedicated fail-safe state management pins on both low and high voltage sides
- VGE real time cycle-by-cycle monitoring

4.3 Safety and regulatory approvals

- Reinforced isolation per DIN V VDE V 0884-10
- Withstand 5000 V rms (1 minute) isolation per UL 1577
- CSA Component Acceptance Notice 5A
- AEC-Q100 grade 1 automotive qualified

5 Ordering information

Table 1. Orderable part variations

Part number[1]	VDD	External clearance and creepage distance[2]	Material (isolation) group[3]	FSISO option (gate state when FSISO is activated)	Temperature (TJ)	Package
MGD3160AM515EK	5.0 V	>7.72 mm	II	Gate ON	−40 °C to 150 °C	32-pin wide body SOIC, 0.65 mm pitch
MGD3160AM518EK	5.0 V	>8.0 mm	I	Gate ON		
MGD3160AM535EK	5.0 V	>7.72 mm	II	Gate 3-STATE		
MGD3160AM538EK	5.0 V	>8.0 mm	I	Gate 3-STATE		
MGD3160AM315EK	3.3 V	>7.72 mm	II	Gate ON		
MGD3160AM318EK	3.3 V	>8.0 mm	I	Gate ON		
MGD3160AM335EK	3.3 V	>7.72 mm	II	Gate 3-STATE		
MGD3160AM338EK	3.3 V	>8.0 mm	I	Gate 3-STATE		

[1] To order parts in tape and reel, add the R2 suffix to the part number. To order parts in tray packing, add the T suffix to the part number.
[2] Per IEC 60950-1 Tables 2K and 2N
[3] Per IEC 60664-1

6 Pinning information

6.1 Pinning

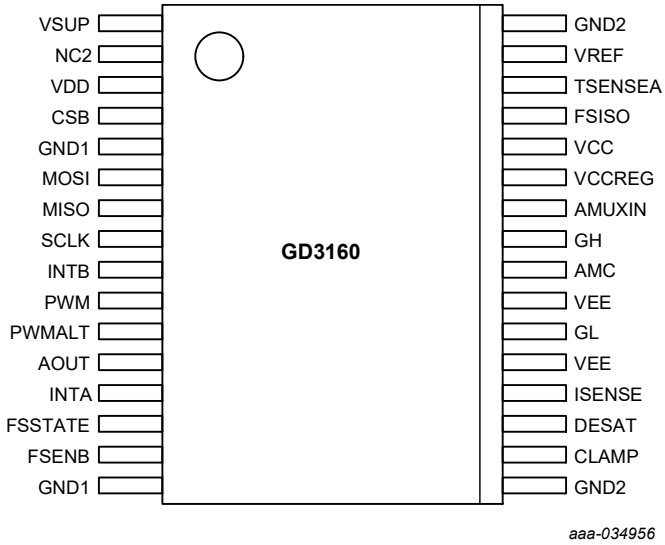


Figure 2. Pin configuration

6.2 Pin description

Table 2. Pin definitions

Pin number	Pin name	Pin type	Definition	Comments
Pins 1 to 16 (low-voltage, non-isolated pins)				
1	VSUP	input / power	Primary power supply for non-isolated low-voltage (LV) domain	Main supply input is compatible with 12 V automotive battery range/transients, referenced to GND1. VSUP may either be (1) driven by 12V, or (2) tied to VDD and powered by an external, post-regulated 3.3 V or 5 V supply.
2	NC2	no connect	No connection	NC2 must be connected to GND1
3	VDD	input-output / power	Power supply for non-isolated low-voltage (LV) logic	Main supply for logic on LV domain, referenced to GND1. VDD may either be (1) regulated internally to 3.3 V or 5.0 V from VSUP, or (2) tied to VSUP and powered by an external, post-regulated 3.3 V or 5 V supply.
4	CSB	input / digital	SPI chip select	Active low CSB activates SPI link and framing
5, 16	GND1	ground 1	Ground for non-isolated (LV) domain power and logic	Redundant GND1 pins provide ground reference for all non-isolated low-voltage (LV) domain signals. Isolated from all circuitry referenced to GND2.
6	MOSI	input / digital	SPI "master-out, slave-in" pin	Input data for GD3160 SPI. MOSI data latches on rising edge of SCLK, MSB first. Internal passive pull down to GND1
7	MISO	output / digital	SPI "master-in, slave-out" pin	Data output for GD3160 SPI. GD3160 outputs MISO on falling edge of SCLK, MSB first.
8	SCLK	input / digital	SPI clock	GD3160 acknowledges SPI clock only when CSB is low. Internal passive pull down to GND1
9	INTB	output / digital	Interrupt / Fault status output	INTB reports fault with active low (logic 0 reports fault). Internal passive pullup to VDD.
10	PWM	input / digital	PWM control command for gate output	Logic high turns on power device gate. PWM pin is ignored during fail-safe, configuration, BIST, reset, and most fault modes. Internal passive pull down to GND1.
11	PWMALT	input / digital	Complementary PWM command for gate output	Complementary PWMALT enforces deadtime constraint and prevents accidental shoot-through condition. Connect to GND1 if unused. Internal passive pull up to VDD .
12	AOUT	output / analog	Duty-cycle encoded output of isolated ADC	5.0 V, 3.9 kHz (or multiplexed with 5.6 kHz) readout is configurable by SPI. Connect high-impedance to GND1 if unused.
13	INTA	output / digital	Interrupt / fault status / monitor	Output pin reports fault via active pulldown interrupt, or reports VCE or VGE state via logic high/low. Pin left open if unused.
14	FSSTATE	input / digital	Fail-safe gate state control pin	Gate output control pin. Connect to GND1 if unused. Internal passive pulldown to GND1.
15	FSENB	input / digital	Fail-safe mode enable pin	Active-low pin enabling fail-safe mode (FSSTATE controls gate). Internal passive pulldown to GND1. Connect to VDD if unused.
Pins 17 to 32 (high-voltage, isolated pins)				
17, 32	GND2	ground 2	Ground for isolated (HV) domain power, analog, and logic	Redundant GND2 pins provide ground reference for all isolated high-voltage (HV) domain. Isolated from all circuitry referenced to GND1. Connect to power device emitter/source.

Table 2. Pin definitions*...continued*

Pin number	Pin name	Pin type	Definition	Comments
18	CLAMP	input / analog	Sense terminal for VCE/VDS overvoltage during turn-off	CLAMP detects Zener breakdown current and increase gate drive impedance and employ soft shutdown for turn-off. Connect to VEE if unused.
19	DESAT	input-output / analog	Drive/sense terminal for VCE/ VDS desaturation condition	Connected to GND2 if unused
20	ISENSE	input / analog	Current sense feedback pin	Resistive network converts current mirror into readable voltage signal on ISENSE. Connect to GND2 if unused.
21, 23	VEE	input / power	Negative gate supply voltage	VEE is the negative voltage on the isolated domain, and is referenced to GND2. Connect to GND2 if a negative supply is not used.
22	GL	output / analog	Pull-down pin for output gate turn-off/discharge event	GL pin pulls gate to VEE
24	AMC	input-output / analog	Direct connect to gate for gate voltage sense and active miller clamp function	AMC provides low-impedance holdoff (active miller clamp) and senses VGE/VGS for reporting and diagnostics.
25	GH	output / analog	Pull-up pin for output gate turn-on event	GH pin pulls gate to VCCREG
26	AMUXIN	input / analog	General-purpose input for isolated ADC	One of many SPI-selectable inputs for the isolated ADC. Connect to GND2 if unused.
27	VCCREG	output / power	Internally-regulated positive gate supply	Programmable gate supply derived from VCC, referenced to GND2. Connect to VCC if unused.
28	VCC	input / power	Positive voltage supply for isolated domain circuitry	Referenced to GND2
29	FSISO	input / digital	HV domain pin to enable the fail-safe state.	Active-high disables PWM, FSSTATE, and turns on GATE.
30	TSENSEA	input / analog	Anode of temp sense diode/NTC of the power module	TSENSEA reads back voltage from temperature sense element, and is referenced to GND2. Includes possible current driver for temp sense network. The temperature sense network cathode should be connected to GND2. Connect to VREF if unused.
31	VREF	output / power	Internally regulated reference voltage for HV domain analog, ADC, and logic	Output for an internally generated 5.0 V, 20 mA regulator. Referenced to GND2

7 Absolute maximum ratings

All voltages are referenced to GND1 or GND2. Currents are positive into and negative out of the specified pins. Exceeding these ratings may cause malfunction or permanent device damage.

Table 3. Absolute maximum ratings

All voltages referenced to GND1 (LV domain) or GND2 (HV domain). Currents are positive into and negative out of the specified pins.

Symbol	Parameter		Min	Max	Unit
Power supplies and current references					
V_{VSUP}	Low voltage domain supply voltage	[1]	−0.3	40	V
V_{VDD3p3}	Low voltage domain logic supply voltage, 3.3 V version	[1]	−0.3	6.0	V
V_{VDD5}	Low voltage domain logic supply voltage, 5.0 V version	[1]	−0.3	6.0	V
V_{VCC}	High voltage domain positive supply voltage	[2]	−0.3	25	V
V_{VEE}	High voltage domain negative supply voltage	[2]	−12	0.3	V
$V_{VCC-VVEE}$	High voltage domain positive/negative supply		−0.3	37	V
V_{VCCREG}	High voltage domain post regulated supply voltage	[2]	−0.3	25	V
I_{VCCREG}	VCCREG output current		—	–100	mA
V_{VREF}	VREF voltage	[2]	−0.3	6.0	V
I_{VREF}	VREF output current		—	–20	mA
Logic pins					
V_{IN}	Logic input pin voltage (FSSTATE, FSENB, PWM, PWMALT, SCLK, CSB, MOSI)	[1]	−0.3	18	V
V_{OUT}	Logic output pin voltage (MISO, INTB, INTA, AOUT)	[1]	−0.3	V_{VDD_max} + 0.3 V	V
V_{FSISO}	Logic input pin voltage (FSISO)	[2]	−0.3	6.3	V
Gate drive output stage					
V_{GH}	GH voltage	[2]	VEE − 0.3	V_{VCCREG_max} + 0.3 V	V
V_{GL}	GL voltage	[2]	VEE − 0.3	V_{VCCREG_max} + 0.3 V	V
V_{AMC}	AMC voltage	[2]	VEE − 0.3	V_{VCCREG_max} + 0.3 V	V
$I_{SOURCEMAX}$	GH max. source Current	[3]	—	–15	A
$I_{SINKMAX}$	GL, AMC max. sink current	[3]	—	15	A
V_{CLAMP}	CLAMP voltage	[2]	VEE − 0.3	V_{VCCREG_max} + 0.3 V	V
V_{DESAT}	DESAT voltage	[2]	−0.3	V_{VCCREG_max} + 0.3 V	V
Temperature sense pin					
$V_{TSENSEA}$	TSENSEA voltage	[2]	−0.3	6.0	V
Interrupt pins					
I_{INTB}	Open drain DC output current	[4]	—	–20	mA
I_{INTA}	Open drain DC output current	[4]	—	–20	mA
ISENSE sense pin					
V_{ISENSE}	ISENSE voltage	[2]	−2.0	V_{VCCREG_max} + 0.3 V	V
AMUXIN pin					
V_{AMUXIN}	AMUXIN voltage	[2]	−0.3	6.0	V
ESD ratings					
V_{ESDHBM}	ESD voltage (HBM) All pins	[5]	 −2.0	 2.0	kV
V_{ESDCDM}	ESD voltage (CDM) Corner pins Other pins	[6]	 −750 −500	 750 500	V
$V_{ESDModule}$	ESD voltage (module level) VSUP, GND1, GND2 pins	[7]	 −8.0	 8.0	kV

Table 3. Absolute maximum ratings...*continued*

All voltages referenced to GND1 (LV domain) or GND2 (HV domain). Currents are positive into and negative out of the specified pins.

Symbol	Parameter	Min	Max	Unit
Immunity				
dV_{ISO}/dt	Common mode transient immunity [8]	—	100	V/ns
PWM frequency				
f_{PWMMAX}	Maximum switching frequency	0	100	kHz

[1] Ref = GND1
[2] Ref = GND2
[3] 50 %, 100 nF, 10 kHz
[4] $V_{INTA, B}$ < 0.8 V
[5] **Human Body Model (HBM) at device level**
ANSI/ESDA/JEDEC JS-001: 2010 Model HBM (human body model)
Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
Test points: pin to GND1 and pin to GND2
[6] **Charged Device Model (CDM)**
ANSI/ESD S5.3.1-2009
ESD Association Standard for Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) - Component Level
[7] **Module Level ESD Tests**
ISO 10605:2008/Cor. 1:2010(E)
Road vehicles – Test methods for electrical disturbances from electrostatic discharge
[8] Pulse width = 10 ns

8 Package information

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 4. Package outline

Package	Suffix	Package outline drawing number
32-pin wide body SOIC	EK	98ARH99137A

8.1 Package outline

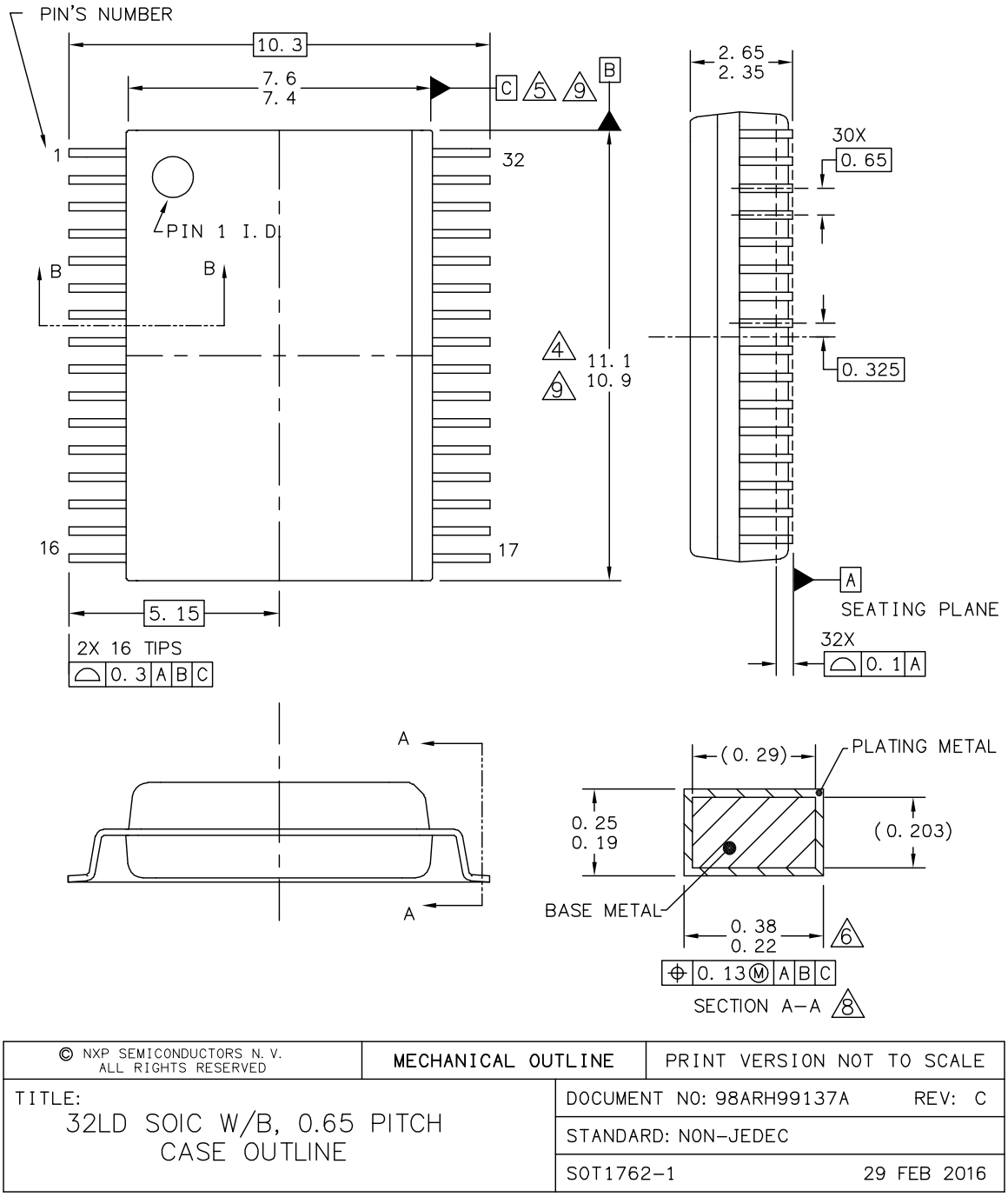
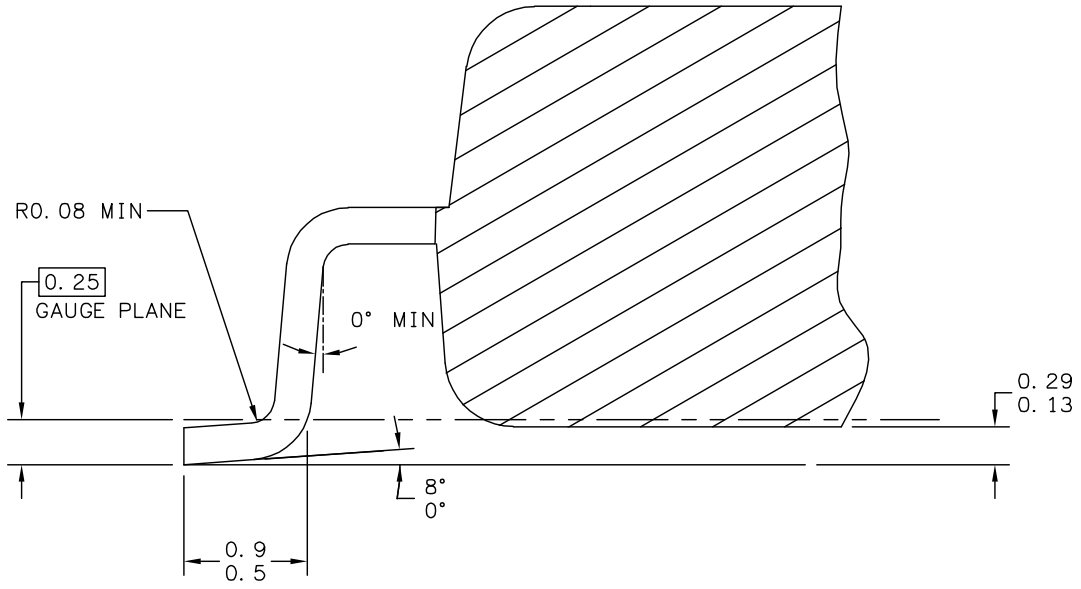


Figure 3. Package outline for SOIC32



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TITLE: 32LD SOIC W/B, 0.65 PITCH CASE OUTLINE	DOCUMENT NO: 98ARH99137A	REV: C
	STANDARD: NON-JEDEC	
	SOT1762-1	29 FEB 2016

Figure 4. Package outline detail for SOIC32

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

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	STANDARD: NON–JEDEC	
	SOT1762–1	29 FEB 2016

Figure 5. Package outline notes for SOIC32

9 Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PB_GD3160 v.2	20230317	Product brief	—	PB_GD3160 v.1.1
Modifications	• Replaced Table 1. • Updated Section 10.			
PB_GD3160 v.1.1	20201012	Product brief	—	PB_GD3160 v.1
Modifications	• Added "and IGBTs" to the document title. • Section 3, updated Figure 1 to include revised application schematic. • Section 4.1, revised "Programmable gate voltage regulator" to "Programmable gate voltage regulator over an expanded range" and revised "5.0 V or 3.3 V I/O available" to "Available in 3.3 V or 5.0 V I/O logic interface variants." • Section 4.2, revised as follows: – Revised "Certified compliant with ISO 26262, supporting ASIL D level functional safety" to "ISO 26262 ASIL D certified supporting ASIL D system level functional safety." – Revised "Current, DESAT, and temperature sense inputs and ADC reporting for IGBT/SiC" to "Ultra-fast, current, DESAT, and temperature sense inputs and ADC reporting for IGBT/SiC." • Section 4.3, revised "Withstand 2500 V rms (1 minute) isolation per UL 1577" to "Withstand 5000 V rms (1 minute) isolation per UL 1577." • Section 5, updated part numbers from "PC33GD3160EK" and "PC33GD3160A3 EK" to "PGD3160AM515EK" and "PGD3160AM315EK." • Removed former Section 6, "Internal block diagram" and all associated content. • Section 6.1, Figure 2, revised the image, updating the pin name "NC" to "NC2" to correspond with the pin name in Table 2. • Section 6.2, revised Table 2. • Section 7, revised as follows: – I_{VCCREG}, revised Max value from "100" to "–100." – I_{VREF}, revised Max value from "20" to "–20." – V_{FSISO}, revised Max value from "12" to "6.3." – $I_{SOURCEMAX}$, revised Max value from "15" ;to "–15." – $I_{SINKMAX}$, revised Max value from "–15" to "15." – I_{INTB} and I_{INTA}, revised Max value from "20" to "–20." • Removed former Section 9, "General functional description" and all associated content.			
PB_GD3160 v.1	20190808	Product brief	—	-

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