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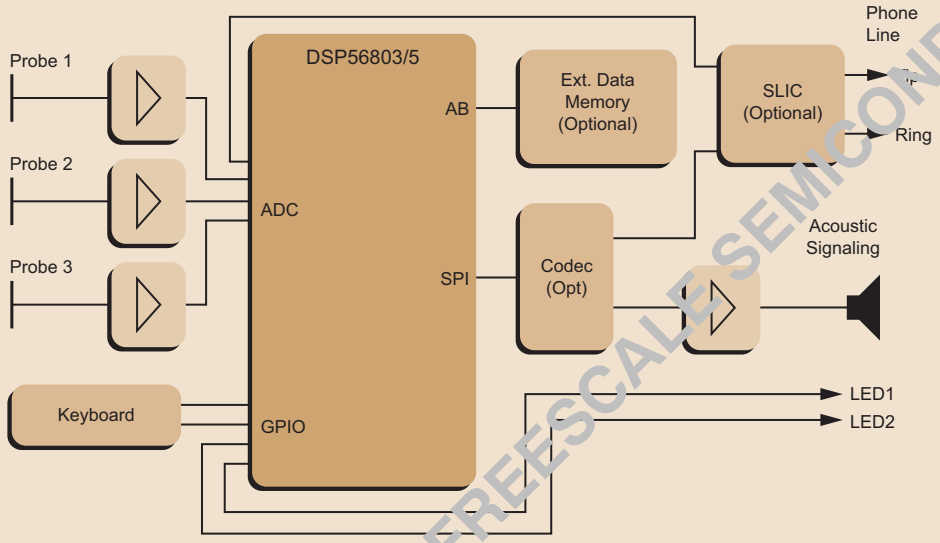
Personal Electrocardiogram (ECG) Monitor

Overview

The cost of a personal electrocardiogram (ECG) monitor can be reduced through use of new technologies that incorporate a digital signal processor (DSP) into one device.

PERSONAL ECG MONITOR USING THE DSP56F803/5



Key Benefits

> Reduces ECG monitor costs by incorporating DSP functions into one device

> ECG monitors can be designed to support real-time evaluation only or with a keypad, display, modem, and external memory for ECG storage

> Supports up to eight probes

> Performs time-multiplexed sampling

> Stores sampled ECG signals using double-buffering technique

> Effective implementation of any of three digital filters

> Out-of-the-box software components designed to expedite time-to-market and reduce development costs

freescale semiconductor

Freescale Ordering Information

Part Number	Product Highlights	Additional Information
DSP56F803	80 MHz, 40 MIPS, CAN, SCI, SPI, ADC, PWMs, Quadrature Decoder, Quad Timer and > 31.5K Program Flash > 512K Program RAM > 4K Data Flash > 2K Data RAM	MCU-friendly instruction set, OnCE for debug, on-chip relaxation oscillator, 2K BootFLASH, external memory expansion, and up to 16 GPIO available in a 100-pin LQFP.
DSP56F805	80 MHz, 40 MIPS, CAN, SCIs, SPI, ADC, PWMs, Quadrature Decoder, Quad Timer and > 31.5K Program Flash > 512K Program RAM > 4K Data Flash > 2K Data RAM	MCU-friendly instruction set, OnCE for debug, on-chip relaxation oscillator, 2K BootFLASH, external memory expansion, and up to 32 GPIO available in a 144-pin LQFP.
DSP56F827	80 MHz, 40 MIPS, SCI, SPI, SSI, TOD, ADC, Quad Timer and > 64K Program Flash > 1K Program RAM > 4K Data Flash > 4K Data RAM	MCU-friendly instruction set, OnCE for debug, external memory expansion, and up to 52 GPIO available in a 128-pin LQFP
MC56F8300 Family	60 MHz, 60 MIPS, up to 576KB Flash, 36KB RAM and Off-Chip Memory, SCI, SPI, ADC, PWM, Quadrature Decoder, Quad Timer, FlexCAN, GPIO, COP/Watchdog, PLL, MCU-style software stack support, JTAG/OnCE for debug, temperature sensor	www.freescale.com
MC56F8100 Family	40 MHz, 40 MIPS, up to 544KB Flash, 32KB RAM and Off-Chip Memory, SCI, SPI, ADC, PWM, Quadrature Decoder, Quad Timer, FlexCAN, GPIO, COP/Watchdog, PLL, MCU-style software stack support, JTAG/OnCE for debug	www.freescale.com
MC56F801x Family	Up to 32 MHz, 32 MIPS, and up to 16KB Flash, 4KB Unified Data/ Program RAM, EEPROM emulation capability, SCI with LIN, SPI, IIC, ADC, PWM, GPIO, COP/Watchdog, MCU-style software stack support, JTAG/OnCE for debug	www.freescale.com

Design Challenges

A personal ECG monitor is a device capable of saving human life. However, its high price limits wider use. A low-cost solution that incorporates digital signal processing into one device can help overcome this obstacle.

Freescale Semiconductor Solution

The diagram on page 1 describes control and digital processing aspects of a proposed solution. The ECG signal is collected by probes located on skin near the heart. The signal is then amplified and read by an analog-to-digital converter (ADC). The quality of the ECG signal depends on the probe's location. This influence can be compensated by using multiple probes in different positions. The number of available ADC channels limits the number of probes. The ADC on the DSP56F803/5 has eight channels. One ADC pin is used to connect to a phone line across a subscriber line interface circuit (SLIC).

The remaining seven pins can be connected to probes. Three probes are considered a common set. Two samples are taken sequentially, while a third is sampled consecutively. The ADC's maximum sampling is 800 kHz. The common sampling frequency of an ECG signal is 500 Hz, leaving an ample reserve to perform time-multiplexed sampling. The ADC resolution is 12-bit, also enough for this purpose.

Double Buffering for Storage and Processing

A sampled ECG signal is stored using a double-buffering technique: one buffer for storage and a second buffer for data processing. After signal processing is completed, filtering, detection of abnormalities, and optional data compression functions are performed. An ECG monitor commonly uses three filters:

> Notch 50/60 Hz

> Band stop 35 Hz, the muscle interference

> High pass 0.5 Hz, drift compensation

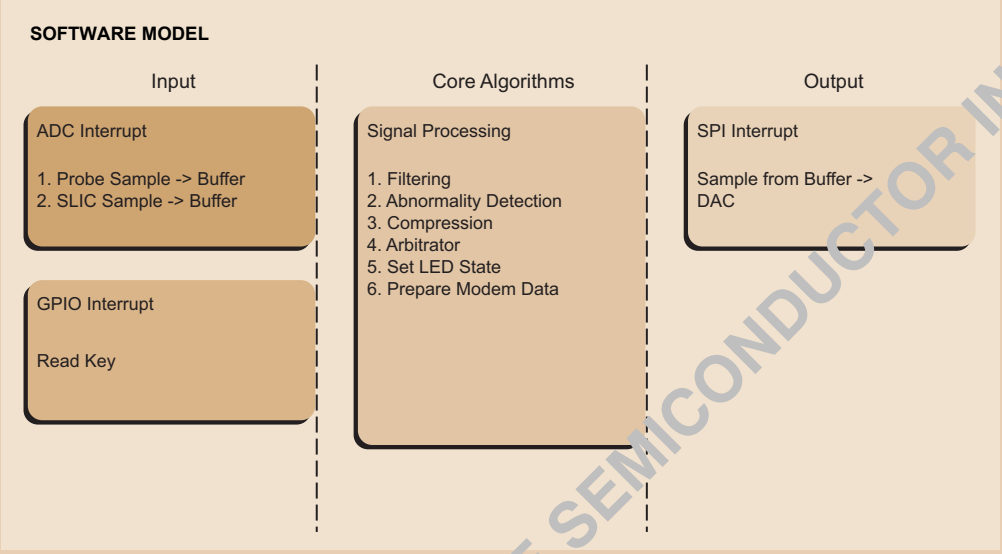
The DSP56F803/5's instruction set is adapted to digital filtering, so any of the filters can be implemented effectively.

ECG Evaluation Method

The ECG can be simply described as a periodic pulse signal, but a wide range of its abnormalities has been described in literature.[1] To simplify ECG evaluation, the difference between measured ECG and reference ECG signals scaled to current beat frequency should be determined. This diagnostic evaluation is not able to classify the type of disorder. The output can take two forms: either a *healthy/diseased* attribute or *continual*, indicating a variable degree of membership to a diseased state. To classify a concrete disorder—for example, an infarction or an arrhythmia—additional criteria must be used based on recognition of pulse shape and detection of parasitic pulses.[1] Inasmuch as the theoretical number of instructions per ECG sample is 40 MIPS/ 500 Hz/3 channels ~ 26000 and the instruction set is adapted to digital signal processing, sufficient reserve exists to perform additional disorder classification.

Verify Disorder Using a Modem

Optionally, the result of classification can be verified by a physician using a modem. The DSP can be connected to a phone line across a SLIC, the internal ADC used at the input side, and the external digital-to-analog converter (DAC) at the output side. The DAC and DSP are connected via the SPI. Modem functions are provided by software. The ECG monitor's software should be programmed in C. The proposed layering of the software and interrupt usage are displayed in the diagram below; Software Model. Individual tasks communicate using semaphores, which are global status variables preventing others from barging in during communication. Modem functions and basic DSP algorithms are components provided by Freescale Semiconductor.



Theoretical Foundations

Assuming maximal ECG frequency is 3 beats per second and 3-channel processing with a sampling frequency of 500 Hz, a process capable of 1500 samples per second and 9 pulses detected per second is required. Using an infinite impulse response (IIR) filter with 6 biquades, about 0.18 MIPS (in SDK implementation) are required to preprocess the ECG signal. Detecting shapes of pulses by correlation with 128-point reference vectors repeating this operation for 10 pulse types, it's possible to perform 3 beats, 3 channels, 10 references = 90 computations of correlation of 128 elements/128 elements vectors, representing about 1.6 MIPS under SDK. In short, about 3 MIPS will be necessary for a basic ECG evaluation, keeping a reserve for time scaling of reference vectors. An additional software modem will require about 6 MIPS in V.22bis implementation (SDK) or about 15 MIPS in V.32bis implementation.

Design Variants

Whole ECG monitors can be designed in several variants: a low-cost variant without a modem and external memory, with real-time evaluation only, and a full variant with keypad, display, modem, and external memory for ECG storage. A variant with external memory must be based on the DSP56F805, because the general purpose input/output (GPIO) pins in the DSP56F803/5 are shared with the external address bus. The GPIO pins are used by a keyboard, for LED signaling, and, optionally, by a display. A keyboard or display can also be connected via the serial communication interface (SCI). To provide connectivity with a personal computer, the SCI can be also used for RS-232 interface.

The functionality of the proposed application design can be demonstrated on evaluation modules DSP56F805EVM or DSP56F803EVM without DAC. These boards contain all required hardware except input analog, probes and amplifiers, and output SLIC.

Development Tools

Tool Type	Product Name	Vendor	Description
Software	CW568X	Freescale Semiconductor	CodeWarrior™ Development Studio for 56800/E Controllers with Processor Expert (Metrowerks)
Software	Processor Expert	Freescale Semiconductor	Software infrastructure that allows development of efficient, high level software applications that are fully portable and reusable across all 56800/E family of processors.
Software	CWDSP56800	Freescale Semiconductor	CodeWarrior Software Development Tools for 56800 (Metrowerks)
Hardware	56F800DEMO	Freescale Semiconductor	56F800 Demonstration Kit
Hardware	DSP56F803EVM	Freescale Semiconductor	Evaluation Module for the 56F803
Hardware	DSP56F805EVM	Freescale Semiconductor	Evaluation Module for the 56F805
Hardware	DSP56F827EVM	Freescale Semiconductor	Evaluation Module for the 56F827
Hardware	MC56F8300DSK	Freescale Semiconductor	56F8300 Developers Start Kit
Hardware	MC56F8367EVM	Freescale Semiconductor	Evaluation Module for the 56F83[illegible]F835x, 56F836x
Hardware	DEMO56F8013	Freescale Semiconductor	Demonstration kit for the 56F80[illegible]
Hardware	DEMO56F8014	Freescale Semiconductor	Demonstration kit for the 56F8014

Reference

1. Online Journal of Cardiology, EKG World Encyclopedia, www.mmip.mcgill.ca/heart/egcw/ecgworld.html.

Disclaimer

This document may not include all the details necessary to completely develop this design. It is provided as a reference only and is intended to demonstrate the variety of applications for the device.

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