Freescale Semiconductor
Addendum

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Errata to MPC885 PowerQUICC Family Reference Manual, Rev. 2

This errata describes corrections to the *MPC885 PowerQUICC Family Reference Manual*, Revision 2. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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Section, Page No.	Changes
General erratum	Replace all instances of the term ‘60x’ with ‘external.’
10.4.1, 10-4	In Figure 10-2, “Internal Memory Map Register (MMR),” change “PARTNUM” reset from “000_0000” to “0000_1001” or “0x09”.
10.4.1, 10-4	In Figure 10-2, “Internal Memory Map Register (MMR)” and Table 10-2, “MMR Field Descriptions,” change bits 0–15 for ISB to 0–13. Bits 14 and 15 are reserved bits and are restricted to containing only a value of 0 to prevent conflicts between the Internal Memory Map and the SEC's memory map.
12.1.2, 12-22	In Table 12-1, “MPC885/MPC880 Signal Descriptions,” add RMII_MII_MDIO to name column of pin P19.
12.1.2, 12-23	In Table 12-1, “MPC885/MPC880 Signal Descriptions,” add RMII2-TXEN [pin T6] description to MII1-TXEN [pin T5] description.
14.2.1, 14-4	In Table 14-1, “The Input Frequency Requirements,” change “320 MHz” to “400 MHz” as follows:

Table 14-1. The Input Frequency Requirements

MODCK[1-2]	Frequency In	PDF	MFI, MFN, MFD for DPGDCK
00, 01	OSCM = 10 MHz to 10.66 MHz	0	160 MHz < OSCLK × 2 × (MFI + (MFN ÷ (MFD+1))) < 400 MHz
11	EXTCLK = 10 MHz to 10.66 MHz	0	160 MHz < OSCLK × 2 × (MFI + (MFN ÷ (MFD+1))) < 400 MHz
10	45 MHz ≤ EXTCLK ≤ 66 MHz	10 MHz ≤ EXTCLK / (PDF+1) ≤ 32 MHz	160 MHz < OSCLK × 2 × (MFI + (MFN ÷ (MFD+1))) / (PDF+1) < 400 MHz

14.3.1.3, 14-13	In the first bullet note dealing with internal clock of 2 x EXTCLK, add the following: “assuming EXTCLK is between 50 MHz to 80 MHz.”
14.3.3, 14-15	In Table 14-6, “TMBCLK Configuration,” change column heading “MF + 1” to say “MFI/(PDF+1).”
14.4.3, 14-17	In the description, “An inductor value of 8.2 Mhz and bypass capacitor values of 0.1 µF and 10 µF provide a two-pole filter with a cutoff frequency of 500 Hz”, change “8.2 MHz” to “8.2 mH”.
14.6.2, 14-21	In Figure 14-13, “PLL and Reset Control Register (PLPRCR),” change ‘0000’ under field PDF to ‘—’ because PDF is not affected by HRESET.
14.6.2, 14-22	In Figure 14-13, “PLL and Reset Control Register (PLPRCR),” and Table 14-9, “PLPRCR Field Descriptions,” change bit field “FIOPD” to “RESERVED”.
15.6.4.7/15-48	In Table 15-19, “AMA/AMB Definition for DRAM Interface,” add the following footnote to “Memory Size” heading: “Memory size takes data bus width into account.”

Section, Page No.	Changes
18.6.1, 18-6	In Table 18-4, “RCCR Field Descriptions,” change bit 12 description to say: “EIE. External interrupt enable. Configure as instructed in the download process of a Motorola-supplied RAM microcode package. 0 DREQ0 cannot interrupt the CP. 1 DREQ0 will interrupt the CP. This bit must be set to enable USB host SOF generation.”
18.6.4, 18-9	In Table 18-7, “CP Command Opcodes,” move USB COMMAND from opcode row 1111 to opcode row 1101.
19.1.2, 19-3	In Table 19-1, “U-Bus Arbitration IDs,” change the term ‘G2 Core’ to ‘PTEC Core’.
21.2.4, 21-10	In Table 21-4, “TODR Field Descriptions,” in TOD field description, change “TOD is cleared automatically after one serial clock...” to say “TOD is cleared automatically after 1 system clock...”
21.3, 21-11	Under third bullet point, change “For an RxBD, the value must be even,” to say, “For an RxBD, the value must be mod 4 aligned.”
27.1, 27-2	In Figure 27-2, “Ethernet Block Diagram,” Clock Generator block: Internal Clock[s] arrows should be reversed; pointing *into* the block, and RCLK and TCLK arrows should be reversed; pointing *out* of the block
31.7.1, 31-9	In Figure 31-5, “USB Controller Operating Modes,” the arrow on the bottom of “Preamble” should point in the opposite direction.
31.7.2, 31-11	In Figure 31-6, “SOF Generation, the “dreq0” signal should point in the opposite direction.
31.7.2, 31-11	In the last paragraph, change to the following: DREQ0 should be configured as external interrupt—bit EIE should be set to 1 in RCCR. When there are no hardware originated requests to the CP, it enters stall state. Configuring DREQ0 as an external interrupt request ensures that only a hardware interrupt request can wake up the host controller.
31.8, 31-12	In Figure 31-7, “USB Parameter RAM Memory Map,” change RSTATE to bold-face type.
31.10, 31-13	In Table 31-4, “Endpoint Parameter Block,” change TSTATE to bold-face type.
31.13.2, 31-28	Modify section to say the following: This command enables the transmission of data from the corresponding endpoint on the USB. This command is expected by the USB controller after a STOP Tx Command, or after transmission error (underrun, time-out, STALL or NAK). To eliminate the USB transmit delay, set STR (start command) in USCOM after launching “RESTART TX” command.”
31.13.2, 31-28	Add the following note to the end of the section:

NOTE

"In Host mode, care should be taken that the RESTART Tx command is not issued during or just before the SOF transmission. To ensure that, the timer's value can be checked."

32.4.3, 32-7 — In Table 32-3, "I2BRG Field Descriptions," change the description for bits 0–7 to read as follows:

"Division ratio 0–7. Specifies the divide ratio of the BRG divider in the I^2C clock generator. The output of the prescaler is divided by $2 \times (DIV + 3 + (2x\ FLT))$, and the clock has a 50% duty cycle. The FLT bit is in the I2MOD register. The minimum value for DIV is 3 if the digital filter is disabled (FLT = 0) and 6 if the digital filter is enabled (FLT = 1)."

33.8, 33-19 — Add a note to beginning of section, as follows: "PIP in transparent mode is not supported."

34.4.1.4, 34-16 — In Figure 34-14, "Port C Special Options Register (PCSO)," change bit 4 to CD3, bit 5 to CTS3, bit 6 to CD4, and bit 7 to CTS4.

35.2.1, 35-3 — First bullet should reference SPS = 0 and second bullet should reference SPS = 1.

42.2.2, 42-3 — Add the following note below the second paragraph:

NOTE

The actual number of active PHY address signals is selected in UTMODE [ADDPIN]; see Section 43.2, "UTOPIA Mode Register (UTMODE)." When a PHY address signal is not activated, the pin reverts to its function as defined by PBDIR alone (UT becomes a don't care). For example, assuming that the UTOPIA interface has been initialized properly, and if only seven PHYs are used in a UTOPIA master application, the SMC1 data signals are still available because RxAddr [3] and TxAddr [3] are not active.

45.2.1, 45-3 — In Table 45-2, "MII and RMII Signals," add '(input)' next to the signal descriptions 'Transmit Clock' and 'Receive Clock'.

45.2.5, 45-7 — In Figure 45-2, "Ethernet Address Recognition Flowchart," the promiscuous mode check at the bottom should indicate when R_CNTRL[PROM] = 0, the state machine leads to False.

45.3.1, 45-12 — Add the following note below Table 45-6, "CPTR RMII Related Field Descriptions":

NOTE

If auto-negotiation is used, then it is recommended to configure RMIIx_RATE_FECx after the PHY has finished the auto-negotiation. The user can then read the line speed from the PHY status registers using MII management frames, and then configure RMIIx_RATE_FECx accordingly.

45.3.2.13, 45-23 — In Figure 45-17, "MII_DATA Register," remove address offset(s) for FEC_2, 0x1E80 and 0x1E82.

Section, Page No.	Changes
45.3.2.13, 45-24	In the last paragraph, add the following: “In the MPC88x or MPC87x, all MII management interface transactions must be done through FEC1 registers. This includes MII_SPEED and MII_DATA registers.”
45.3.2.14, 45-24	In Figure 45-18, “MII_SPEED Field Descriptions,” remove address offset(s) for FEC_2, 0x1E84 and 0x1E86.
Appendix B	Added content to Appendix B, “Serial Communications Performance,” as follows:

Appendix B
Serial Communications Performance

Due to the architecture of the MPC885 family, the overall performance of the serial channels cannot be stated in absolute terms. The serial channels of the MPC885 family can be programmed in many different modes, which require different degrees of processing. There may be several individual bottlenecks in the system, with their own specific considerations. These are described in the following sections.

B.1 Serial Clocking (Peak Rate Limitation)

The maximum rate at which a serial channel can be clocked is governed by the synchronization hardware of the serial channels. The rate at which the serial channel can be clocked depends on the physical interface of the channel. Examples include:

- Maximum clocking rate for an SCC connected to a dedicated set of pins (NMSI mode) = SYNCCLK/2
- Maximum clocking rate for the TDM channel = SYNCCLK/2.5

For limitations of other channels, refer to the appropriate chapter of the manual.

SYNCCLK is a programmable clock rate which is derived from the system frequency; see Chapter 14, “Clocks and Power Control.” At its maximum rate, it is equal to the system frequency.

The maximum serial clock rate is a limitation on the peak data rate. This is the maximum rate at which the receiver or transmitter hardware can transfer data between its internal FIFO and the serial line. However, this rate is higher than the rate at which data in these internal FIFOs can be processed by the CPM and transferred to system memory. Therefore, this peak rate can only be maintained for short bursts which do not exceed the internal FIFO depth. The serial clocks must also be turned off between these bursts. The FIFOs of the SCCs are 32 bytes for SCC1 and 16 bytes for SCC[2–4]. The SMCs and SPI are double-buffered, and thus have an effective FIFO depth of two characters.

To summarize, the architecture of the MPC885 family allows the serial channels to handle high-speed bursts of data for short periods of time subject to their internal FIFO sizes. If transfers are sufficiently short, and if serial clocks are turned off between the transfers, then these individual transfers can be performed at up to the peak rate. Over time, however, the average amount of data transferred must not exceed the average CPM processing rate.

If any of the conditions outlined above are not satisfied, then the rate at which the serial channels are clocked must not exceed the rate at which the CPM can process data from them. In other words, the average rate limitation must also be treated as the peak rate limitation.

The I^2C channel is the only exception to these rules. Its maximum serial transfer rate is limited by its hardware, not by the rate at which the CPM services it. At its maximum transfer rate, it will only consume 25% of the CPM bandwidth.

B.2 Bus Utilization

Given the width and clock speed of the system bus of the MPC885 family , bus utilization is not a critical system limitation, considering the data rates supported by the MPC885 family. Specifically, the peak system bus transfer rate of a 80 MHz MPC885 family (using single-beat transfers to zero wait-state memory) is 1200 Mbps, whereas the maximum aggregate serial data rate supported at that frequency is usually less than 50 Mbps.

However, whereas bus utilization is not a major consideration, bus latency can be. Extreme periods of bus latency could potentially cause a FIFO to overrun or underrun. Where this is a more critical issue, some specific recommendations are made. For example, recommendations for system bus latency are made for an MPC860MH operating in QMC mode; see the *QMC Supplement to MC68360 and MPC860 User's Manuals*.

B.3 CPM Bandwidth (Average Rate Limitation)

The communications processor module (CPM) is a single shared resource used by all of the serial channels. It handles low-level protocol processing tasks and manages DMA for all of them. In the architecture of the MPC885 family, the CPM is the central communications processing engine, to which the individual serial controllers (SCC, SMC, SPI, I^2C, and PIP) make requests for service. Therefore, the serial channels must not request more service than the CPM can provide; else, FIFO underrun or overrun errors will result.

The amount of processing required by a particular serial channel depends on the mode in which the channel is configured, and the maximum rate at which the channel requests service. [While this rate is usually equivalent to the serial clocking rate, under certain conditions the serial clocking rate could be higher; this is because the FIFOs of the serial channels can provide a 'local averaging' effect on the data rate, and thus can handle short bursts. See Section B.1, "Serial Clocking (Peak Rate Limitation)."

B.3.1 Performance of Serial Channels

The table provided in this section lists the data rates supported by the CPM for particular channels in different modes. These figures assume that the serial channel in question is the only channel in operation. Individual channels operating at the data rate quoted would consume 100% of the CPM bandwidth.

The performance available from different serial channels in different protocols varies greatly. This is due to the amount of overall processing required by the protocol and by the split between hardware-assist provided in the serial channel and processing performed in the CPM by microcode. For example:

- An SCC in UART mode provides more processing in the SCC hardware, whereas an SMC in UART mode is more reliant on the CPM. Therefore, the performance of an SCC in UART mode is greater.

- An SCC in HDLC mode performs most of the processing (e.g. bit manipulation, deframing) in hardware, whereas HDLC processing for QMC channels falls on the communications processor module (CPM). Thus, an SCC in HDLC mode can process more data than an SCC in QMC mode, even if all QMC time slots are concatenated into one logical channel.

Maximum data rates are given for most channels as full duplex. Channels operating in half duplex will require only half the CPM service, and thus the maximum data rates supported for these channels doubles.

Managing DMA for the serial channels is a significant portion of the CPM processing. Therefore, because channels with larger frame sizes require the CPM to access the buffer descriptors less often, these channels experience higher performance. An example of this shown in the table below is an SCC in HDLC mode; a channel with a minimum frame size of 64 bytes has better performance than one with a minimum frame size of 5 bytes.

The performance figures listed in Table B-1. are for a 25 MHz system clock only. In general, performance scales linearly with frequency; an MPC885 family with a 50-MHz system clock would support twice the quoted data rate. Thus, a combination of serial channels and protocols which are beyond the MPC885 family's performance scope at 25 MHz may be possible at 50 MHz.

Performance figures quoted in Table B-1 assume worst-case conditions. Worst-case conditions are a steady stream of minimum-size frames. Furthermore, for the SCC in QMC mode, it assumes that all virtual channels simultaneously reach end-of-frame, and thus all must close and open buffers simultaneously.

Table B-1. MPC885 Family Serial Performance at 25 MHz

Protocol	Speed [see note 2]
SCC in transparent	8 Mbps FD
SCC in HDLC (5 byte minimum frame size)	8 Mbps FD
SCC in HDLC (64 byte minimum frame size)	11 Mbps FD
SCC in UART	2.4 Mbps FD
SCC in Ethernet	22 Mbps HD
SCC in Ethernet	11 Mbps FD
SCC in QMC mode	2.1 Mbps FD
SCC in BISYNC	1.5 Mbps FD
SCC in asynchronous HDLC/IrDA	3 Mbps FD
SMC in transparent	1.5 Mbps FD
SMC in UART	220 Kbps FD
I^2C	520 Kbps [see note 1]
SPI (16 bit)	3.125 Mbps
SPI (8 bit)	500 Kbps
PIP (8 bit width)	625 Kbyte/s
PIP (16 bit width)	1250 Kbyte/s
SCC in SS#7 [optional RAM microcode]	6 Mbps FD

Table B-1. MPC885 Family Serial Performance at 25 MHz

Protocol	Speed [see note 2]
SCC in SS#7 [optional RAM microcode] [without scrambling]	8 Mbps FD
SCC in SS#7 [optional RAM microcode] [with scrambling]	5.5 Mbps FD

Notes:

1. I^2C is a special case. Its performance is limited by its hardware, not by the CPM. An I^2C port operating at 520 Kbps would consume only 25% of the CPM bandwidth of an MPC885 family device operating at 25 MHz.
2. Performance scales linearly with system frequency.
3. FD indicates full-duplex; HD indicates half-duplex.
4. Ethernet full and half duplex modes are quoted separately merely to highlight the feature.
5. SPI is inherently full-duplex, and it is therefore not necessary to mark it as so.

B.3.2 IDMA Considerations

Although the IDMA channels are implemented in microcode by the CPM, they need not necessarily be calculated into the CPM bandwidth. If IDMA is not a time-critical task, then its priority can be programmed to be the lowest of the CPM tasks. If this is done, IDMA is treated as a background task and serviced only when other channels do not require service.

If IDMA is configured to be a higher-priority task, then its transfers must be considered when calculating demands on the CPM bandwidth. Table B-2 provides performance information for the IDMA channels in their different modes. Its use is similar to the table provided for the serial channels (Table B-1.).

Table B-2. IDMA Performance at 25 MHz

Protocol	Speed
IDMA memory to memory	5.7 MByte/s
IDMA memory to memory with burst aligned source/dest address	10.4 MByte/s
IDMA dual address, peripheral to memory	2.2 MByte/s
IDMA dual address, memory to peripheral	1.6 MByte/s
IDMA single address, peripheral to memory	5 MByte/s
IDMA single address, memory to peripheral	5 MByte/s

Notes:

1. Performance scales linearly with device operating frequency.
2. IDMA transfer rates are independent of bus cycle length.

B.3.3 Performance Calculations

Special configurations verified by experiment.

The performance figures quoted in Table B-1. can be used to estimate the overall CPM bandwidth required in a particular system configuration. To calculate the total system load, add the CPM utilization from every channel together. Assuming approximately linear performance versus frequency, the general problem reduces to taking simple ratios:

$$\text{CPM Utilization} = \left(\frac{\text{serial rate}_1}{\text{max serial rate}_1}\right) + \left(\frac{\text{serial rate}_2}{\text{max serial rate}_2}\right) \cdots$$

For example, because a 25-MHz MPC885 family device running Ethernet (theoretically) at 22 Mbps consumes approximately 100% of the CPM bandwidth, what bandwidth does a (practical) 10-Mbps channel require?

$$\text{CPM Utilization} = \frac{\text{serial rate}}{\text{max serial rate}} = \frac{10}{22} = 0.45$$

The above equation shows the 10-Mbps channel requiring 45% of the CPM bandwidth of a 25-MHz MPC885 family device.

A spreadsheet tool for performing serial performance calculations has been developed and is available on the world-wide web site at http://www.freescale.com. It is entitled “CPM Performance Spreadsheet”.

- Please note that CPM load estimation is a linear approximation to a somewhat nonlinear phenomenon, and cannot be relied upon to be exact. When performance estimations approach the maximum loading (i.e. greater than approximately 95%), the user should test the system on target hardware to determine the exact load. Conversely, some system configurations that calculate to greater than 100% by these equations have been verified by experiment. These include the following:A 25-MHz MPC885 family device with one half-duplex Ethernet and 24 QMC channels (that is, 24 x 64 kbps QMC) [if and only if SCC1 is Ethernet and QMC channels are spread over two SCCs, for example, SCC1=Ethernet, SCC2=QMC channels 0–11, SCC3=QMC channels 12-23].
- A 33 MHz MPC885 with one half-duplex Ethernet and 32 QMC channels (that is, 32 x 64 kbps QMC) [if and only if SCC1 is Ethernet QMC channels are spread over two SCCs, for example, SCC1=Ethernet, SCC2=QMC channels 0-15, SCC3=QMC channels 16–31].
- A 40-MHz MPC885 family device with four half-duplex Ethernet channels.

More examples of CPM bandwidth calculations follow:

Example #1:

MPC885v (at 25 MHz) operating 1 × 10 Mbps Ethernet in half duplex, 1 × 2 Mbps HDLC, 1 × 64 Kbps HDLC, 1 × 9.6 Kbps UART and 1 × 38 Kbps SMC UART. The following equation applies:

$$\left(\frac{10}{22}\right) + \left(\frac{2}{8}\right) + \left(\frac{0.064}{2.4}\right) + \left(\frac{0.0096}{2.4}\right) + \left(\frac{0.038}{0.22}\right) = 0.89 \qquad (<1)$$

This yields a percentage CPM utilization of 89% meaning the device can handle these protocols at this frequency. Note the 9.6-Kbps UART link only requires 0.4% of the CPM bandwidth, implying that in any configuration where there is free bandwidth that it will be possible to run a low-rate UART link.

Example #2:

MPC885 family device (at 25 MHz) running 24 QMC channels with an additional 2 HDLC channels operating at 128 Kbps each. The following equation applies:

$$\left(\frac{2 \times 0.128}{8}\right) + \left(\frac{24 \times 0.064}{2.1}\right) = 0.76 \qquad (<1)$$

Example #3:

The MPC885 family device (at 25 MHz) running 32 QMC channels and one additional 2 Mbps HDLC channel. The following equation applies:

$$\left(\frac{2}{8}\right) + \left(\frac{32 \times 0.064}{2.1}\right) = 1.22 \qquad \text{(will not work)}$$

Because the result above is greater than one, this will not work with a 25-MHz MPC885 family device. However, if the system clock is increased to 33 MHz, CPM utilization drops below 1, allowing example #3 to be supported. The following equation applies:

$$1.22 \times \left(\frac{25}{33}\right) = 0.92 \qquad (<1)$$

Example #4:

MPC885 family device (at 25 MHz) with a block of data transferred by IDMA at 512 Kbytes/s to a 32-bit peripheral, one asynchronous HDLC at 1Mbps, one UART at 9,600 baud, and one transparent channel at 2 Mbps.

$$\left(\frac{0.512}{5} + \frac{1}{3} + \frac{0.0096}{2.4} + \frac{2}{8}\right) = 0.69$$

In the case of IDMA, this process calculates the peak CPM utilization, not the sustained rate. By nature, IDMA transfers occur at random intervals and are not consistent bit rates when compared to the serial channel operation.

Example #5:

MPC885 family device (at 40 MHz) with three Ethernet channels at 10 Mbps and one UART at 9,600 baud.

$$\left(\frac{3 \times 10}{22} + \frac{0.0096}{2.4}\right) = \left(\frac{1.37 \times 25}{40}\right) = 0.85$$

B.4 ATM Performance

This appendix provides receiver and transmitter performance information for the MPC885 family.

The information was gathered under the following conditions:

- System clock = 50 MHz
- AAL5 – Buffer (data) size > 200 bytes
- AAL0 – Interrupt per BD

- Average load on external bus
- System memory is DRAM with 5-2-2-2 performance at 50 MHz.

NOTE

CPM performance is theoretically linear to the system clock. However, a slow external memory or an overloaded PPC bus can degrade the performance figures.

ATM performance is also influenced by the number of PHYs and the timer 4 rate for the APC. The more PHYs are serviced with the APC or the higher the timer 4 rate is configured, the less the maximum bit rate for ATM can be. Please contact your Freescale representative for more information.

B.5 Receiver

Table B-3 shows the UTOPIA and serial ATM receiver performance of the MPC885 family when configured with internal and external connection tables.

Table B-3. Receiver Performance (with 50-MHz System Clock)

Mode	Condition	Performance (in Mbps)	
		UTOPIA	Serial (3)
Internal Channels	AAL5, middle frame, look-up table (1)	89	27/19
	AAL0, no CRC10, look-up table (1)	68	24/17.5
	AAL5, middle frame, address comp (2)	84	26/18
	AAL0, no CRC10, address comp (2)	65	23/17
External Channels	AAL5, middle frame, address compression	69	23/18
	AAL0, Address compression	50	21/17
	AAL5, middle frame, CAM	84	27/19
	AAL0, CAM	57	24/17.5
External AAL5 + MPHY	AAL5, middle frame, Address compression	66	NA

Note:

1. Cell header located in the middle of the look-up table (16th place), AAL0 RCT[NCRC] is set.
2. Address compression with FLMASK and SLMASK containing 4 lsb zeros.
3. No scrambler / With Scrambler and coset

Table B-4 allows for calculating the impact of several modes on performance.

Table B-4. Additional Features Load

Mode	Numerator	Denominator (CPM Load in Mbps)
MCF set	Total RX bit rate	1678
CRC-10 (in AAL0 channel)	Total bit rate of AAL0 channels with CRC10	457

Table B-4. Additional Features Load (continued)

Mode	Numerator	Denominator (CPM Load in Mbps)
PM on internal channel	Total bit rate of internal channels with PM	694
PM on external channel	Total bit rate of external channels with PM	419
Statistics mode activated, single PHY	Total RX bit rate	2870
Statistics mode activated, multy PHY	Total RX bit rate	1340

Example:

The following load exists:

- 10 AAL0 internal channel, each receives 5Mbps.
- 2 AAL5 internal channels, 10Mbps each, and one of the channels has PM on.
- What is the overall CPM load?
  - the load caused by the AAL0 channels = total_AAL0_rate/max_AAL0_rate = (10*5)/68 = 50/68
  - the load caused by the AAL5 channels = total_ALL5_rate/max_AAL5_rate = (2*10)/89
  - the load caused by the PM processing = 10/694
  - overall load = 50/68 + 20/89 + 10/694 = 0.97 < 1

We see that in the PM load, the numerator contains only the bit rate that carries PM (only 1 AAL5 channel performs PM hence only 10 Mbps).

The overall bit rate came out less than one. This means that the CPM is able to handle the calculated load.

If in addition to the previous channels configuration, MCF is also activated, the new CPM load would yield:

- the load caused by MCF = total_channel_rate/MCF_max_rate = (10*5+2*10)/1678

And the overall load is 0.97 + 70/1678 = 1.01

This time the overall load is higher than one. This means that we have exceeded the CPM capacity. This can be resolved by various ways: raising the system clock, improving external memory, or cancelling some of the traffic.

B.6 Transmitter

Table B-5 shows the UTOPIA and serial mode transmitter performance of the MPC885 family when configured with internal and external connection tables.

Table B-5. Transmitter (Including 1 Priority APC) Performance (with 50 MHz System Clock)

Mode	Condition	Mbit	
		UTOPIA [4]	Serial [5]
Internal Channels	AAL5, middle frame + APC	57/69	32/23
	AAL0 +APC	51/60	28/20.5
External Channels	AAL5, middle frame + APC	47/51	27/20
	AAL0 + APC	43/47	24/19
External AAL5 + MPHY	2 MPHYs with similar bitrate	44/48	NA
	1 fast MPHY and 1 slow [1]	43	NA
	1 fast MPHY and 1 slow [2]	41	NA
	1 fast MPHY and 3 slow [3]	38	NA

Note:

1. In case of one 25Mbit PHY and 1 XDSL 1Mbit. This example is for N=4 for the first PHY and N=0.16 for the second.
2. In case of one 25Mbit PHY and 1 XDSL 500 Kbit. This example is for N=1 for the first PHY and N=0.02 for the second.
3. In case of one 25Mbit PHY and 3 XDSL 500 Kbit. This example is for N=1 for the first PHY and N=0.02 for the second.
4. APC(N=1)/APC(N=4). In case of N=4, UTOPIA mode, the numbers represent the CP load, but a 100% load cannot be achieved if the CP works solely on transmit. For example if an AAL0 internal channel operates at 30Mbps and APC(N=4) this means that the CP is half loaded. A full CP load that would yield a 60Mbps is not reachable. This is because of the UTOPIA TX implementation which requires the CP to wait for the UTOPIA to finish transmitting a cell before it passes it a new cell.
5. No scrambler / With Scrambler and coset

Table B-6 allows for calculating the impact of several modes, on performance.

Table B-6. Performance Calculation

Mode	Numerator	Denominator (CPM Load in Mbps)
PM on internal channel	Total bit rate of internal channels with PM activated	575
PM on external channel	Total bit rate of external channels with PM activated	457
CRC-10 on AAL0 Tx channel	Total bit rate of CRC-10 AAL0 channels	207
Statistics mode set, single PHY	Total transmitted bit rate	2237
Statistics mode set, multy PHY	Total transmitted bit rate	1342

Example of mixed transmit receive CPM load calculation:

- 2 transmit external AAL5 channels, each of them is 6Mbps.
- One of the two TX AAL5 channels has PM activated.
- 5 receive, internal channels, address compression, AAL0, each of them is 4Mbps.

- MCF is on.
- 2 Tx AAL5 load = (2*6)/47
- PM load = 6/457
- 5 Rx AAL0 channels = (5*4)/65
- MCF load = (5*4)/1678
- overall CPM load = 12/47 + 6/457 + 20/65 + 20/1678 = 0.6

End of Appendix B

Appendix F, F-1	Under the first bullet, remove the sentence, “The time-slot assigner is not implemented.”
F.1, F-1	Add “PCMCIA Port A only” to bullet “The MPC875 supports one PCMCIA channel.”
F.2 F, F-2	Add NOTE at end of section:“MPC875 supports PCMCIA Port A only.”
F. 2.2, F-4	Add the following to the list of Other Unimplemented Signals: CE1_B, CE2_B, and ALE_B.

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