

MSC8156 Mezzanine Detailed Design Specification

1 Overview

1.1 Scope

This document provides a detailed design description of the MSC8156 Mezzanine card. It also describes the architecture, interconnections, and used components.

1.2 References

The documents listed below are referenced in this document:

1. MSC8156 Reference Manual
2. MSC8156 Hardware Specification
3. PICMG AMC.0 R2.0 “Advanced Mezzanine Card Base Specification”
4. PICMG AMC.2 “PCIe Advanced Mezzanine Card Base Specification”
5. PICMG AMC.4 “SRIO Advanced Mezzanine Card Base Specification”
6. Freescale 815x Power Calculator

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1.3 Definitions, Acronyms, and Abbreviations

Table 1. Definitions, Acronyms, and Abbreviations

AMC	Advanced Mezzanine Card (AdvancedMC™)
ATCA	Advanced Telecommunications Computing Architecture
BDM	Background Debug Mode
CPLD	Complex Programmable Logic Device
DIP	Dual In Line Package
DNP	Do Not Populate
DSP	Digital Signal Processor
EEPROM	Electrically Erasable Programmable Read Only Memory
GETH	Giga-bit Ethernet
HSC	High Speed Connector
HW	Hardware
I ² C (bus)	Inter-Integrated Circuit
RCW	Reset Configuration Word
sRIO	Serial Rapid IO
UART	Universal Asynchronous Receiver/Transmitter
UEC	UCC Gigabit Ethernet Controller
MTCA	Micro Telecommunications Computing Architecture (MicroTCA™)

2 MSC8156 Mezzanine

The MSC8156 Mezzanine is a MSC8156 based daughter card that can be plugged into the Freescale Common AMC base card. The mezzanine is populated with the MSC8156 and DDR3 memory. All active interfaces, such as SRIO, Ethernet, control, clocking, and power are routed to the high-speed connector (HSC), that connects the mezzanine to the AMC base card.

For high-bandwidth operation, the MSC8156 routes two ×4 3.125 GHz SRIO interfaces (SRIO0 and SRIO1) to the HSC. The SRIO1 interface can be configured as an option to support PCIe.

Control and data traffic are handled by two RGMII interfaces, which are routed from the MSC8156 to the HSC.

Auxiliary functions like reset/control/GPIO/timer and clocking are routed to the HSC. These are connected to the generic mezzanine control bus on the AMC base card, which in turn connects to the system FPGA. The FPGA drives the reset and control of the MSC8156 mezzanine. Power is provided to the card through the HSC connector. All voltages are generated from the base card.

Figure 1 shows the MSC8156 mezzanine architecture.

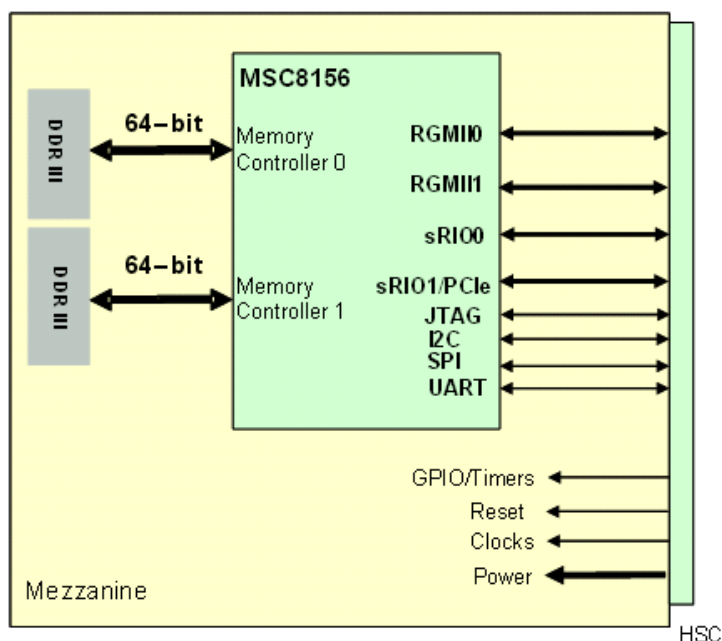


Figure 1. MSC8156 Mezzanine Architecture

3 Features

- Target use
 - Mezzanine card for AMC base card
 - Software development platform for baseband, media gateway, and RNC solutions
 - Design reference and enablement platform for customers and third parties
- Form factor
 - 70mm × 39mm
- Connectivity
 - 1× SRIO interfaces (×4) connected to the HSC
 - 1× SRIO/PCIe multiplexed interface (×4) connected to the HSC
 - 2× RGMII interfaces connected to the HSC
 - 2× DDR3 interfaces each with 512 Mbytes of 64-bit DDR3 memory
 - I²C interface for boot connected to the HSC
 - UART connected to the HSC
 - SPI Interface
- Debug
 - JTAG connected to the HSC
 - JTAG header provided for DSP mezzanines on AMC base card
 - Multiple test points

Features

- Power supply (provided by base card)
 - 3.3V IO
 - 2.5V Ethernet
 - 1.5V/0.75V DDR3
 - 1.0V Core
 - 1.0V SerDes
- Clocks
 - SerDes, Ethernet provided by AMC base card
 - Core clock on mezzanine

3.1 SerDes Interface

The high-speed serial interface contains two Lynx blocks that supports several SerDes interfaces on the MSC8156. The MSC8156 mezzanine implements following options:

- **Option 1:** Lynx0 = SRIO0 [×4], Lynx1 = SRIO1 [×4]
- **Option 2:** Lynx0 = SRIO0 [×4], Lynx1 = PCIe [×4]

In the Lynx1 hardware block, the SRIO1 and PCIe signals are multiplexed onto the same MSC8156 pins; option 1 uses the SRIO1 interface, while option 2 uses the PCIe. Note that SRIO and PCIe specifications use different termination schemes. SRIO uses 0.1-μF DC blocking capacitors at the receiver end, while PCIe uses a 0.1μF DC blocking capacitors at the transmitter end. This option is selectable by a number of capacitor/resistor changes at the board assembly stage.

3.1.1 SRIO Interface

The MSC8156 supports two RapidIO controllers. Each supports a high-performance, point-to-point, low pin count packet, switched-level interconnect that can be used in a variety of applications as an open standard. The MSC8156 SRIO subsystem complies with the RapidIO interconnect specification revision 1.2. Each port controller supports ×1 or ×4 width at 1.25, 2.5, and 3.125 GHz.

The MSC8156 mezzanine routes the two ×4 SRIO interface to the HSC for distribution to the AMC base card.

[Table 2](#) described the connections between the MSC8156 and the HSC.

Table 2. MSC8156 SRIO Interface

Signal	IO	Comment
SRIO Controller 0		
SRIO0_TXD0_P	O	Direct connection to HSC
SRIO0_TXD0_N	O	Direct connection to HSC
SRIO0_TXD1_P	O	Direct connection to HSC
SRIO0_TXD1_N	O	Direct connection to HSC
SRIO0_TXD2_P	O	Direct connection to HSC

Table 2. MSC8156 SRIO Interface (continued)

Signal	IO	Comment
SRIO0_TXD2_N	O	Direct connection to HSC
SRIO0_TXD3_P	O	Direct connection to HSC
SRIO0_TXD3_N	O	Direct connection to HSC
SRIO0_RXD0_P	I	DC blocking capacitor at MSC8156 pin
SRIO0_RXD0_N	I	DC blocking capacitor at MSC8156 pin
SRIO0_RXD1_P	I	DC blocking capacitor at MSC8156 pin
SRIO0_RXD1_N	I	DC blocking capacitor at MSC8156 pin
SRIO0_RXD2_P	I	DC blocking capacitor at MSC8156 pin
SRIO0_RXD2_N	I	DC blocking capacitor at MSC8156 pin
SRIO0_RXD3_P	I	DC blocking capacitor at MSC8156 pin
SRIO0_RXD3_N	I	DC blocking capacitor at MSC8156 pin
SRIO0_REFCLK_P	I	DC blocking capacitor at MSC8156 pin
SRIO0_REFCLK_N	I	DC blocking capacitor at MSC8156 pin
SRIO0_IMP_CAL_TX	I	TX Impedance calibration control (100 to ground)
SRIO0_IMP_CAL_RX	I	RX impedance calibration control (200 to ground)
SRIO Controller 1		
SRIO1_TXD0_P	O	Direct connection to HSC
SRIO1_TXD0_N	O	Direct connection to HSC
SRIO1_TXD1_P	O	Direct connection to HSC
SRIO1_TXD1_N	O	Direct connection to HSC
SRIO1_TXD2_P	O	Direct connection to HSC
SRIO1_TXD2_N	O	Direct connection to HSC
SRIO1_TXD3_P	O	Direct connection to HSC
SRIO1_TXD3_N	O	Direct connection to HSC
SRIO1_RXD0_P	I	DC blocking capacitor at MSC8156 pin
SRIO1_RXD0_N	I	DC blocking capacitor at MSC8156 pin
SRIO1_RXD1_P	I	DC blocking capacitor at MSC8156 pin
SRIO1_RXD1_N	I	DC blocking capacitor at MSC8156 pin
SRIO1_RXD2_P	I	DC blocking capacitor at MSC8156 pin
SRIO1_RXD2_N	I	DC blocking capacitor at MSC8156 pin
SRIO1_RXD3_P	I	DC blocking capacitor at MSC8156 pin
SRIO1_RXD3_N	I	DC blocking capacitor at MSC8156 pin

Table 2. MSC8156 SRIO Interface (continued)

Signal	IO	Comment
SRIO1_REFCLK_P	I	DC blocking capacitor at MSC8156 pin
SRIO1_REFCLK_N	I	DC blocking capacitor at MSC8156 pin
SRIO1_IMP_CAL_TX	I	TX impedance calibration control (100 to ground)
SRIO1_IMP_CAL_RX	I	RX impedance calibration control (200 to ground)

To operate at 3.125, 2.5, or 1.25 GHz, the MSC8156 uses a fixed LVDS SerDes clock frequency of 125 MHz, which is provided by SRIOx_REFCLK from the AMC base card.

The transmission frequency of the MSC8156 SRIO should match the reset configuration word SCLK bits.

3.1.2 PCIe

The MSC8156 supports a PCI express controller that supports communication with PCIe devices. The PCIe interface is designed to comply with the PCI express specification, Revision 1.0a.

Table 3 gives details of PCIe signals (for clarity, the SRIO multiplexed signal are also included in the table).

Table 3. PCIe Signals

Signal	IO	Multiplexed with	Comments
PE_TXD0_P	O	SRIO1_TXD0_P	DC blocking capacitor at MSC8156 pin
PE_TXD0_N	O	SRIO1_TXD0_N	DC blocking capacitor at MSC8156 pin
PE_TXD1_P	O	SRIO1_TXD1_P	DC blocking capacitor at MSC8156 pin
PE_TXD1_N	O	SRIO1_TXD1_N	DC blocking capacitor at MSC8156 pin
PE_TXD2_P	O	SRIO1_TXD2_P	DC blocking capacitor at MSC8156 pin
PE_TXD2_N	O	SRIO1_TXD2_N	DC blocking capacitor at MSC8156 pin
PE_TXD3_P	O	SRIO1_TXD3_P	DC blocking capacitor at MSC8156 pin
PE_TXD3_N	O	SRIO1_TXD3_N	DC blocking capacitor at MSC8156 pin
PE_RXD0_P	I	SRIO1_RXD0_P	Direct connection to HSC
PE_RXD0_N	I	SRIO1_RXD0_N	Direct connection to HSC
PE_RXD1_P	I	SRIO1_RXD1_P	Direct connection to HSC
PE_RXD2_N	I	SRIO1_RXD2_N	Direct connection to HSC
PE_RXD3_P	I	SRIO1_RXD3_P	Direct connection to HSC
PE_RXD3_N	I	SRIO1_RXD3_N	Direct connection to HSC
SRIO1_REFCLK_P	I	–	DC blocking capacitor at MSC8156 pin
SRIO1_REFCLK_N	I	–	DC blocking capacitor at MSC8156 pin

For PCIe, the MSC8156 requires a fixed LVDS SerDes clock frequency of 100 MHz which is provided by SRIOx_REFCLK from the AMC base card.

3.1.3 Termination Scheme

To accommodate both PCIe and SRIO on the Lynx 1 interface, the termination scheme in Figure 1 is used. When Lynx 1 is configured as SRIO (option A), 0.01- μ F blocking capacitors are placed at the receive end and 0 resistors at the transmit end. When Lynx 1 is configured as PCIe (option B) 0.1- μ F blocking capacitors are placed at the transmit end and 0 resistors at the receive end. By default, Lynx 1 is configured as SRIO.

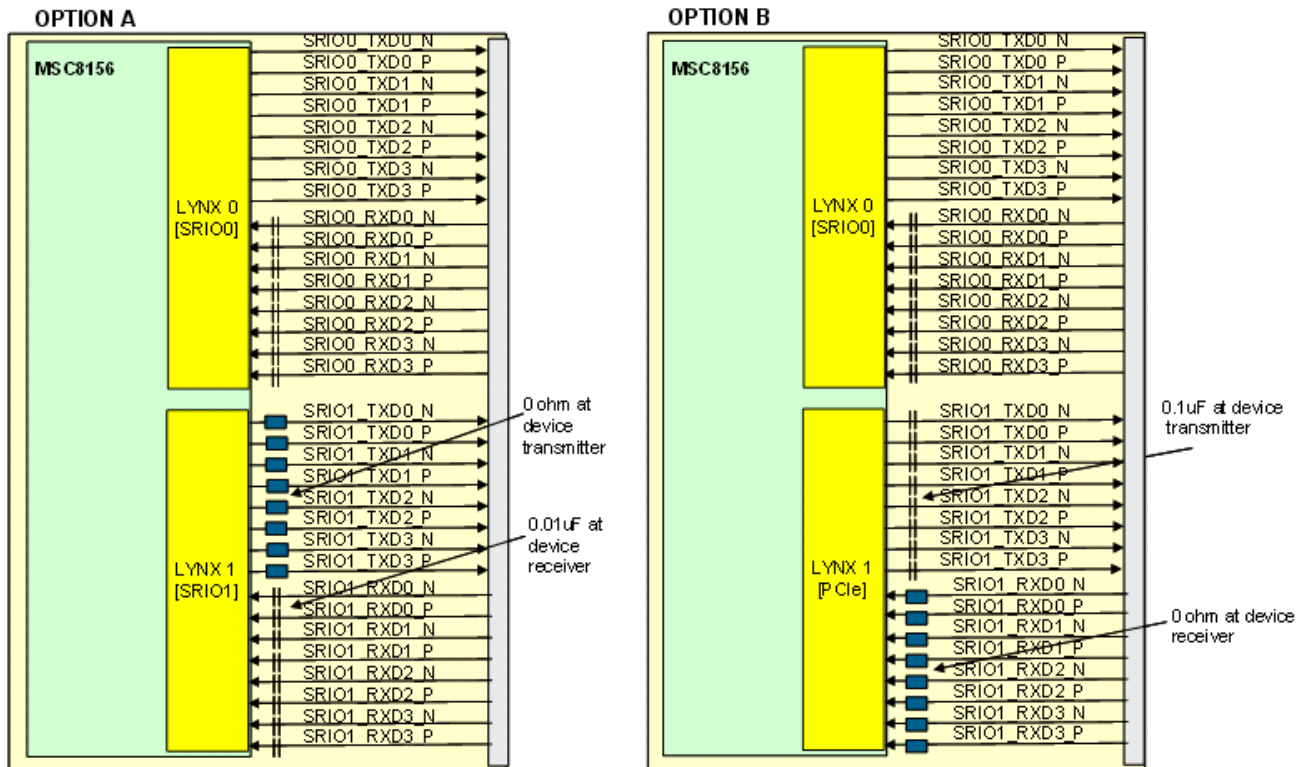


Figure 2. SerDes Termination Scheme

3.2 Ethernet Interface

The MSC8156 supports two UCC gigabit Ethernet controllers (UECs) that are coordinated by the QUICC engine controller. The UEC interfaces on the MSC8156 is configured to use the RGMII interface. Note that the option to use SGMII is not available, because the SerDes pins have been allocated for SRIO use.

Both controllers RGMII interfaces are connected to the HSC; these signals are described in Table 4 and Figure 3. Typically a source termination value of 22 is placed at the transmitter pins (depending on board simulation).

Table 4. MSC8156 Ethernet Interface

Signal	IO	Comments
Ethernet Controller 1		
GE1_TX_CLK	I	Direct connection to HSC
GE1_TX_CLK	O	Direct connection to HSC through source termination
GE1_GTX_CTL	O	Direct connection to HSC through source termination
GE1_TXD0	O	Direct connection to HSC through source termination
GE1_TXD1	O	Direct connection to HSC through source termination
GE1_TXD2	O	Direct connection to HSC through source termination
GE1_TXD3	O	Direct connection to HSC through source termination
GE1_RX_CLK	I	Direct connection to HSC
GE1_RX_CTL	I	Direct connection to HSC
GE1_RXD0	I	Direct connection to HSC
GE1_RXD1	I	Direct connection to HSC
GE1_RXD2	I	Direct connection to HSC
GE1_RXD3	I	Direct connection to HSC
Ethernet Controller 2		
GE2_TX_CLK	I	Direct connection to HSC
GE2_GTX_CLK	O	Direct connection to HSC through source termination
GE2_TX_CTL	O	Direct connection to HSC through source termination
GE2_TXD0	O	Direct connection to HSC through source termination
GE2_TXD1	O	Direct connection to HSC through source termination
GE2_TXD2	O	Direct connection to HSC through source termination
GE2_TXD3	O	Direct connection to HSC through source termination
GE2RX_CLK	I	Direct connection to HSC
GE2RX_CTL	I	Direct connection to HSC
GE2RXD0	I	Direct connection to HSC
GE2RXD1	I	Direct connection to HSC
GE2RXD2	I	Direct connection to HSC
GE2RXD3	I	Direct connection to HSC
MDIO		
GE_MDC	O	Unused (nc)
GE_MDIO	B	Unused (nc)

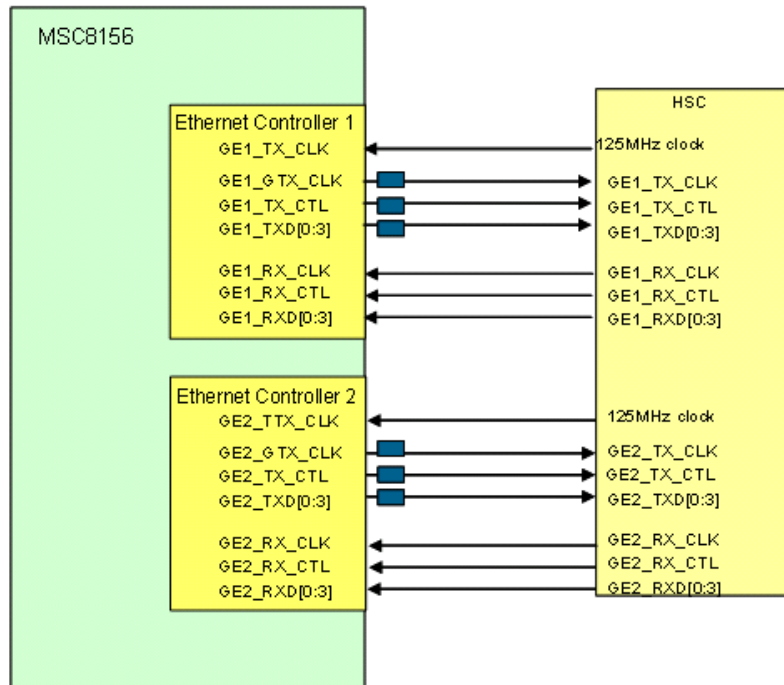


Figure 3. Ethernet Interface

3.3 MSC8156 DDR-3

Each MSC8156 supports dual 64-bit DDR3 controllers. The design utilizes both memory controllers attaching 512 Mbytes DDR3 memory to each. The 512 Mbytes are made of four 800 MHz, 8-Mbytes \times 16 bits \times 8 banks (1-Gbit) devices. The part used for this design is the Micron MT41J64M16BLA-15E.

The DDR3–SDRAM is configured with 13-row address lines, 10-column address lines, and 8 banks. Control of each memory device is done through CS0 signal. Individual differential clocks and their associated enable signal are routed to each memory. Note that EEC is not supported in this configuration.

Every DDR3 signal is a member of one of four separate groups. Each group has unique rules in terms of signal connection and signal routing. The four groups and the connectivity between controller and memory are shown in [Table 5](#).

Table 5. DDR3 Signals

Signal Group	MSC8156 Signal	DDR3 Device1 Signal	DDR3 Device 2 Signal	DDR3 Device 3 Signal	DDR3 Device 4 Signal	Termination /Notes	Description
Address and Command	MA[12:0]	A[12:0]	A[12:0]	A[12:0]	A[12:0]	47 Ω to VTT	Address bus
	MBA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	47 Ω to VTT	Bank address bus
	MWE	WE	WE	WE	WE	47 Ω to VTT	Write enable
	MCAS	CAS	CAS	CAS	CAS	47 Ω to VTT	Column address strobe
	MRAS	RAS	RAS	RAS	RAS	47 Ω to VTT	Row address strobe

Table 5. DDR3 Signals (continued)

Signal Group	MSC8156 Signal	DDR3 Device1 Signal	DDR3 Device 2 Signal	DDR3 Device 3 Signal	DDR3 Device 4 Signal	Termination /Notes	Description
Control	MCKE0	CKE	CKE	CKE	CKE	47 Ω to VTT	Clock enable
	MCKE1					47 Ω to VTT	Clock enable
	MCS0	CS	CS	CS	CS	47 Ω to VTT	Chip select
	MODT0	ODT	ODT	ODT	ODT	47 Ω to VTT	On-Die termination
	MODT1					47 Ω to VTT	On-Die termination
	Data	MDQS0±	LDQS±				ODT
MDQS1±		UDQS±				ODT	Data strobes/complement
MDQS2±			LDQS±			ODT	Data strobes/complement
MDQS3±			UDQS±			ODT	Data strobes/complement
MDQS4±				LDQS±		ODT	Data strobes/complement
MDQS5±				UDQS±		ODT	Data strobes/complement
MDQS6±					LDQS±	ODT	Data strobes/complement
MDQS7±					UDQS±	ODT	Data Strobes/complement
MDM0		LDM				ODT	Data mask
MDM1		UDM				ODT	Data mask
MDM2			LDM			ODT	Data mask
MDM3			UDM			ODT	Data mask
MDM4				LDM		ODT	Data mask
MDM5				UDM		ODT	Data mask
MDM6					LDM	ODT	Data mask
MDM7					UDM	ODT	Data mask
MDQ[7:0]		DQ[7:0]				ODT	Data bus
MDQ[15:8]		DQ[15:8]				ODT	Data bus
MDQ[23:16]			DQ[7:0]			ODT	Data bus
MDQ[31:24]			DQ[15:8]			ODT	Data bus
MDQ[39:32]				DQ[7:0]		ODT	Data bus
MDQ[47:40]				DQ[15:8]		ODT	Data bus
MDQ[55:48]					DQ[7:0]	ODT	Data bus
MDQ[63:56]					DQ[15:8]	ODT	Data bus
Clocks	MCK[1:0]±	MCK0±	MCK0±	MCK0±	MCK0±		Clock/complement

Table 5. DDR3 Signals (continued)

Signal Group	MSC8156 Signal	DDR3 Device1 Signal	DDR3 Device 2 Signal	DDR3 Device 3 Signal	DDR3 Device 4 Signal	Termination /Notes	Description
Misc	ZQ					240 Ω to VSSQ (GND)	
		RESET	RESET	RESET	RESET	1.5V tolerant	Device reset

Complex DDR3 timing adaptation is available through the DDR clocking subsystem of the MSC8156, and it supports the following:

- Positioning of the DQS output during writes to DDR memory
- Sampling of input data from DDR memory
- Synchronizing the incoming DDR data to the internal clock
- Control of the relationship between output data and CLK_OUT
- Write leveling
- Read leveling
- ZQ calibration

3.3.1 Terminations and I/O Voltage

The DDR3 interface operates with 1.5 V I/O and 0.75 VTT voltages, which are supplied from the AMC base card.

3.3.2 MSC8156 Mezzanine Memory Mapping

Table 6 describes the MSC8156 mezzanine memory map.

Table 6. MSC8156 Mezzanine Memory Map

Address Range	Memory Type	Size
0x40000000–0x5FFFFFFF	External DDR3 Bank 1	512 Mbytes
0x60000000–0x7FFFFFFF	Reserved	512 Mbytes
0x80000000–0x9FFFFFFF	External DDR3 Bank 2	512 Mbytes
0xA0000000–0xBFFFFFFF	Reserved	512 Mbytes
0xC0000000–0xC0107FFF	M3 memory	1 Mbyte + 32 Kbyte
0xC0108000–0xFECFFFFFFF	Reserved	511 Mbyte – 32 Kbyte
0xFED00000–FEDFFFFFFF	MAPLE-B	1 Mbyte
0xFEE00000–0xFEE3FFF	QUICC Engine Subsystem	256 Kbytes
0xFEE40000–0xFEEFFFFF	Reserved (QUICC engine subsystem)	768 Kbytes

Table 6. MSC8156 Mezzanine Memory Map (continued)

Address Range	Memory Type	Size
0xFE000000–0xFE007FFF	Boot ROM	96 Kbytes
0xFE008000–0xFFFFFFFF	Reserved	928 Kbytes

3.4 MSC8156 UART Interface

The MSC8156 UART is connected directly to the HSC.

Table 7. MSC8156 UART Interface

Signal	IO	Comments
UTXD	O	Multiplexed with GPIO29
URXD	I	Multiplexed with GPIO28

3.5 MSC8156 JTAG Interface

The MSC8156 EONCE module allows non intrusive interaction with the SC3850 core, enabling examination/analysis of registers, memory, and on-chip peripherals. The EONCE module connects with the debugging system through the on-chip JTAG TAP controller pins.

The MSC8156's EONCE JTAG debug ports are connected directly to the HSC. The EEO signal is used to drive the cores into debug, while the EE1 indicates if a core is in debug. The EONCE signals available on the HSC connector are described in [Table 8](#).

Table 8. MSC8156 JTAG Interface

Signal	IO	Comments
EE0	I	Direct connection to HSC
EE1	I	Connected to test point
TMS	I	Direct connection to HSC
TRST	I	Direct connection to HSC
TCK	I	Direct connection to HSC
TDI	I	Direct connection to HSC
TDO	O	Direct connection to HSC

3.6 Reset and Configuration Signals

3.6.1 Reset

The MSC8156 has three external reset sources as follows:

- Power on Reset (PORESET)
- Hard Reset (HRESET)

- Soft Reset (SRESET).

Assertion of the PORESET signal starts the power on reset flow, the MSC8156 reads its reset configuration word (RCW) and the PLL locks. Assertion of the open drain (OD) HRESET resets the individual blocks and registers, but not the PLL. The SRESET is not used in this design and is pulled high.

Table 9 shows the MSC8156 Reset Signals.

Table 9. MSC8156 Reset Signals

Signal	IO	Comments
PORESET	I	Direct connection to HSC
HRESET	OD	Connected to HSC using a 10K pull up (to 3.3V)
SRESET	I	Not used, 10K pull up to 3.3V

3.6.2 Configuration

PORESET is the high-level reset of the MSC8156, and when asserted, it drives all other resets within the MSC8156. The rising edge of PORESET is used by the MSC8156 to latch external RCW signals.

The RCW source (RCW_SRC[0:2]) option enables the MSC8156 to load the RCW from a variety of sources. These signals are driven from the FPGA on the AMC base card.

The 2 RCW_ source options in Table 10 are used in the design. These are selectable through switches on the base card.

Table 10. Reset Configuration Signals

RCW_SRC[0:2]	Description	Comment
010	Load RCW from I ² C	Standard operation
100	Hardcode option 1	For factory programming

The hard-coded option is used during factory board bring up. By default the MSC8156 loads the RCW from I²C.

To enable multi-DSP boot over I²C, the MSC8156's STOP_BS and GPIO[0:1] signals are routed to the FPGA, which in turns uses them to control the multi-DSP boot process.

All the configuration signals are connected directly to the HSC and routed on the base card to the FPGA that drives the configuration and control signals. When the reset configuration flow is complete, the signals revert to their default GPIO settings.

Table 11 shows the Reset Configuration Connections.

Table 11. Reset Configuration Connections

Signal	IO	Reset	Post Reset Configuration
RCW_SRC0	B	Reset source	GPIO27/TMR 4
RCW_SRC1	B	Reset source	GPIO25/TMR 2

Table 11. Reset Configuration Connections (continued)

Signal	IO	Reset	Post Reset Configuration
RCW_SRC2	B	Reset source	GPIO24/TMR 1
STOP_BS	B	Multi-DSP I ² C control	–
GPIO0	B	Multi-DSP I ² C control,	GPIO0
GPIO1	B	Multi-DSP I ² C control,	GPIO1

Figure 4 shows the RCW Control.

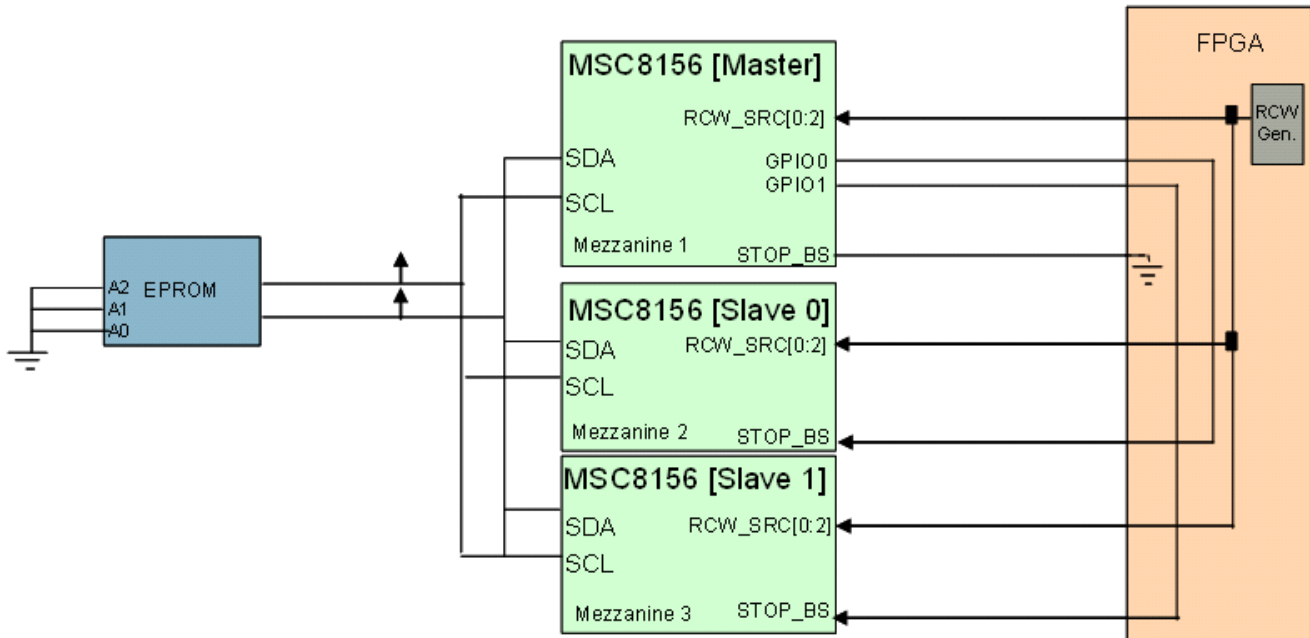


Figure 4. Reset Configuration Word Control

3.6.2.1 Loading Reset Configuration Word from External I²C

When the load RCW from I²C option is selected, the board powers up and samples the RCW_SOURCE pins and reads 010 for I²C. The MSC8156 then accesses the I²C bus at address B[7:0]= b1010000, which represents the EEPROM. Bits B[7:4] = b1010 are hard coded into the EEPROM device, while the bits B[3:1] are defined by the A[2:0] pins, which are tied low. The final bit B0 is set by the read/write signal.

Table 12. EEPROM Address

Signal			A[2:0] pins			R/W	
B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

After the master MSC8156 (DSP1) has read its RCW, it configures itself as a slave EEPROM using the address b1010111. The slaves, DSPs, then access DSP1 to read their RCW.

The I²C EEPROM is programmed by DSP1, with the RCW described in [Table 13](#) and [Table 14](#). These are the default values and can be changed by the user when required.

Table 13. RCWLR (Load from I²C)

RCWLR Bit	Name	Value	Description
[31:30]	CLKO	01	Source is PLL1 [CLKOUT=100 MHz]
29	–	0	Reserved
28:24	S2P	00011	SerDes Port 0: Rapid IO 4 × 3.125 GHz
23:20	S1P	0011	SerDes Port 1: Rapid IO 4 × 3.125 GHz
19:18	–	00	Reserved
17	SCLK2	1	SerDes reference clock = 125 MHz
16	SCLK1	1	SerDes reference clock = 125 MHz
15:8	–	0	Reserved
7	PLL1DIS	0	PLL1 enabled (required for Clock Mode 0)
6	–	–	Reserved
5:0	MODCK	000000	Clock Mode 0

DSP1: RCWLR=0x43330000

DSP2: RCWLR=0x43330000

DSP3: RCWLR=0x43330000

Table 14. RCWHR (Load from I²C)

RCWLR Bit	Name	Value	Description
[31:30]	RES	00	Reserved
29	EWDT	0	Disable watch dog timer
28	PRDY	0	PCI Express not ready
27:24	BPRT	0001	Boot Port=SRIO with no I ² C support
23	RIO	1	Host access after boot, enabled
22	RPT	0	RIO pass through disabled
21	RHE	0	RapidIO controller is agent
20:19	–	00	Reserved
18	RM	1 0 0	DSP1: Reset Master DSP2: Reset Slave DSP3: Reset Slave
17:13	–	00000	Reserved
12	GE1	1	RGMII selected
11	GE2	1	RGMII selected
10	R1A	0	Do not accept all device IDs
9	R2A	0	Do not accept all device IDs

Table 14. RCWHR (Load from I²C) (continued)

RCWLR Bit	Name	Value	Description
8:3	Device ID	000000 000001 000010	DSP1 = 000000 DSP2 = 000001 DSP3 = 000010
2	–	0	Reserved
1	RMU	0	Access local memory Port 0
0	CTLS	1	Common transport type is a large system
DSP1: RCWHR=0x01841801 DSP2: RCWHR=0x01801809 DSP3: RCWHR=0x01801811			

3.6.2.2 Loading Reset Configuration Word from Hard-Coded Option

When the MSC8156 is configured to load the hard-coded RCW, that is, RCW_SRC[0:2] = b100, it is initialized with the hard-coded RCW as described in [Table 15](#) and [Table 16](#).

Table 15. RCWLR (Hard Coded)

RCWLR Bit	Name	Value	Description
[31:30]	CLK	00	Source is PLL0 [CLKOUT=80 MHz]
29	–	0	Reserved
28:24	S1P	01010	SerDes port 1, PCIe 1x SGMII1. SGMII2
23:20	S2P	0011	SerDes port 0, Rapid IO 4x 3.125 GHz
19:18	0	00	Reserved
17	SCLK2	1	SerDes ref clock = 125 MHz
16	SCLK1	1	SerDes ref clock = 125 MHz
15:6	–	0000000000	Reserved
5:0	MODCK	000000	Clock mode 0
DSP1: RCWLR=0x0A330000 DSP2: RCWLR=0x0A330000 DSP3: RCWLR=0x0A330000			

Table 16. RCWHR (Hard Coded)

RCWLR Bit	Name	Value	Description
[31:30]	–	00	Reserved
29	EWDT	0	Disable watch dog timer
28	PRDY	0	PCIe not ready
27:24	BPRT	0000	Boot port is SRIO (BPRT value ignored)
23	RIO	1	Host access after boot, enabled

Table 16. RCWHR (Hard Coded) (continued)

RCWLR Bit	Name	Value	Description
22	RPT	0	RIO pass through disabled
21	RHE	0	RapidIO controller is host
20:19	–	00	Reserved
18	RM	0	Not reset master
17:13	–	00000	Reserved
12	GE1	1	RGMI selected
11	GE2	1	RGMI selected
10	R1A	0	SRIO0 does not accept all device IDs
9	R2A	0	SRIO1 does not accept all device IDs
8:3	Device ID	000000	Device ID=0
2	–	0	Reserved
1	RMU	0	Access local memory port 0
0	CTLS	1	Common transport type is a large system
DSP1: RCWHR=0x00801801 DSP2: RCWHR=0x00801801 DSP3: RCWHR=0x00801801			

3.7 I²C Interface

The I²C bus can be used to load RCW and boot code from the I²C. The bus is connected to an EEPROM on the AMC base card. [Table 17](#) describes the connections.

Table 17. I²C Signals

Signal	IO	Comment
SDA	B	I ² C data line, direct connection to HSC
SCL	B	I ² C clock line, direct connection to HSC

3.8 Clocking

All MSC8156 internal frequencies are derived from the 100 MHz on-board clock (CLKIN) and the clock mode which is defined in the RCW. A CLKIN of 100 MHz and clock mode 0 sets the six MSC8156 cores to 1 GHz. The CLKOUT signal is connected to a test point that depends on the boot mode, as shown in [Table 14](#) and [Table 16](#).

Table 18 shows the clocking frequencies for clock mode 0.

Table 18. Clocking Frequencies for Clock Mode 0

Block	Frequency (MHz)
CLKIN	100
PLL0	900
PLL1	1000
PLL2	800
CLASS	500
DSP core subsystem	1000
HSSI	333
QUICC engine	500
MAPLE	450
DDR controller 1	800
DDR controller 2	800

3.9 SPI Interface

The serial peripheral interface (SPI) allows the exchange of data with other devices containing SPI. In this case, the MSC8156 is connected to a 16-Mbyte external flash (Spansion S25FL128P) located on the AMC base card by the SPI bus. The large memory gives the MSC8156 the option to boot stand-alone with stored application code. The SPI bus is connected to the flash memory through FPGA. This gives the user the choice of using the pins as GPIO if the SPI option is not used.

Table 19 and Figure 5 shows SPI interface signals.

Table 19. SPI Interface

MSC8156 Signal	IO	Comment
SPI_SL	I	Multiplexed with GPIO20
SPI_MISO	OD	Multiplexed with GPIO19
SPI_MOSI	OD	Multiplexed with GPIO18
SPI_SCK	OD	Multiplexed with GPIO17

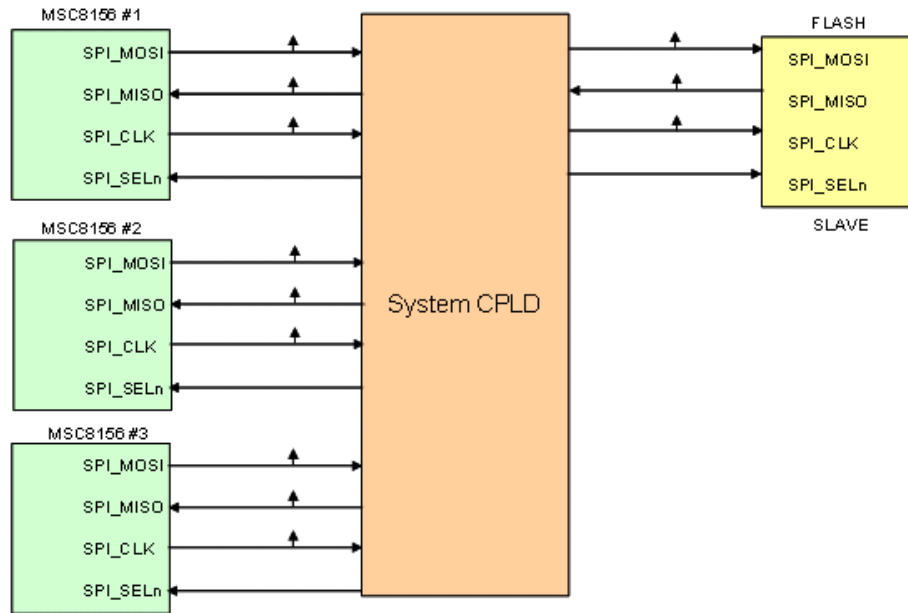


Figure 5. SPI Interface

3.10 GPIO/Timers and Interrupts

A number of GPIO, timers, and interrupts are routed to the HSC. These are connected directly to the AMC base card's FPGA, and can be configured as required. Note that some of these signals are multiplexed with the reset configuration signals. Once the reset is complete, the signals revert to the GPIO/Timer/Interrupt option.

Table 20. GPIO/Timer and IRQ Signals

Signal	IO	Comment
GPIO0/IRQ0	B	Used for I ² C Boot control
GPIO1/IRQ1	B	Used for I ² C Boot control
GPIO17	B	Multiplexed with SPI_SCK
GPIO18	B	Multiplexed with SPI_MOSI
GPIO19	B	Multiplexed with SPI_MISO
GPIO20	B	Multiplexed with SPI_SL
GPIO24/TMR1	B	Multiplexed with RCW_SRC2
GPIO25/TMR2	B	Multiplexed with RCW_SRC1
GPIO27/TMR4	B	Multiplexed with RCW_SRC0
GPIO28	B	Multiplexed with UART_RXD
GPIO29	B	Multiplexed with UART_TXD
GPIO30	B	Multiplexed with I ² C_SCL
GPIO31	B	Multiplexed with I ² C_SDA

Two non-maskable interrupts are routed to the FPGA through HSC.

Table 21. Non-Maskable Interrupts

Signal	IO	Comment
INT_OUT	O	Direct connection to HSC
NMI	I	Direct Connection to HSC

3.11 Power

The MSC8156 mezzanine is supplied with power from the AMC base card. The power requirements are application dependent. The user should refer the MSC8156 power calculator for the mezzanine power requirements. [Table 22](#) details the voltage split.

Table 22. Power Requirements

Signal	Power (W)	Current (A)	Voltage	Comment
MSC8156				
[VCORE] VDD VDDPLL0 VDDPLL1 VDDPLL2 VDDSDXC VDDSDXP	See 8156 Power Calculator [ref 6]		1.0V	Internal Logic Power System PLL 0 - Low impedance System PLL 1 - Low impedance System PLL 2 - Low impedance
[VSERDES] VDDRIOPLL VDDSDXC VDDSDXP			1.0V	SERDES PLL - Low impedance SERDES C Power - Low impedance SERDES P Power - Low impedance
VDDDD			1.5V	DDR3 Controller 1 DDR3 Controller 2
MVREF			0.75V	DDR3 tracking
VDDIO			2.5V	General IO
VDDGE1 VDDGE2			2.5V	Eth. Controller 1 Eth. Controller 2
DDR3 (MT41J64M16 x 8)				
VDD	2768mW	1845mA	1.5V	DDR3 IO
VTT	529mW	705mA	0.75	1uA leakage on reference voltage

The DDR3 power is calculated using the following:

DDR 3 VTT/Vref Calculation (0.75V)

Per Memory Controller: Address and Control Lines = 22 lines (0.75V/47W = 16 mA per Line) = 22 × 16mA = 352mA

Biasing is assumed to be negligible.

Per MSC8156 Mezzanine = $352\text{mA} \times 2 = 704\text{mA}$

DDR3 1.5V calculation

From Micon Power calculator per “×16 bit” device = 346mW

Per MSC8156 Mezzanine = $346\text{ mW} \times 8 = 2768\text{ mW}$

The ripple requirements on the rails are described in [Table 23](#).

Table 23. Voltage Ripple Requirements

Voltage (V)	1.0V	1.5V	2.5V
MSC8156	0.97V (−3%) => 1.05V (+5%)	±75mV (±5%)	±125mV (±5%)
DDR3	–	± 75mV (±5%)	–

The DDR3 reference voltage VTT (0.75V) should track the 1.5V. Both the 1.5V and the 0.75V are supplied from the AMC base card.

The HSC has a 1.1A per pin rating. [Table 24](#) describes the number of power pins used at the HSC connector to supply power.

Table 24. MSC8156 Mezzanine Power Pins

Voltage (V)	Number of Pins Allocated	Comments
0.75V	3	DDR3 /2 (VTT)
1.0V	14	Core
1.0V	3	SERDES
1.5V	6	DDR3
2.5V	4	From Ethernet IO supply
2.5V	2	From VIO Supply (3.3V or 2.5V)

For power sequencing, MSC8156 Core (1.0V) should rise first followed by the 2.5V IO.

3.11.1 PLL Power Supply Design

Each of the MSC8156 PLL blocks has an external RC filter for the PLLn_AVDD signals. Refer the MSC8156 data sheet for used filtering scheme.

3.12 Mezzanine Connector

The HSC provides connectivity and power between the AMC base card and the mezzanine. The connector has 150 pins with 1.1A current rating plus an integrated ground.

The connector pin out is described in [Table 25](#). The SAMTEC QTS high-speed header connector is used. The header mates with a Samtec QSS high-speed socket on the AMC base card.

Table 25. High-Speed Connector Pin Definition

MSC8156				HSC			
Pin No.	IO	V	Signal Name	Pin No.	IO	V	Signal Name
1	–	0	GND	2	–	0	GND
3	O	–	SD0_TXD0_P	4	I	–	SD0_RXD0_P
5	O	–	SD0_TXD0_N	6	I	–	SD0_RXD0_N
7	–	0	GND	8	–	0	GND
9	O	–	SD0_TXD1_P	10	I	–	SD0_RXD1_P
11	O	–	SD0_TXD1_N	12	I	–	SD0_RXD1_N
13	–	0	GND	14	–	0	GND
15	O	–	SD0_TXD2_P	16	I	–	SD0_RXD2_P
17	O	–	SD0_TXD2_N	18	I	–	SD0_RXD2_N
19	–	0	GND	20	–	0	GND
21	O	–	SD0_TXD3_P	22	I	–	SD0_RXD3_P
23	O	–	SD0_TXD3_N	24	I	–	SD0_RXD3_N
25	–	0	GND	26	–	0	GND
27	I	–	SD0_REFCLK_P	28	I	–	SD1_REFCLK_P
29	I	–	SD0_REFCLK_N	30	I	–	SD1_REFCLK_N
31	–	0	GND	32	–	0	GND
33	O	–	SD1_TXD0_P	34	I	–	SD1_RXD0_P
35	O	–	SD1_TXD0_N	36	I	–	SD1_RXD0_N
37	–	0	GND	38	–	0	GND
39	O	–	SD1_TXD1_P	40	I	–	SD1_RXD1_P
41	O	–	SD1_TXD1_N	42	I	–	SD1_RXD1_N
43	–	0	GND	44	–	0	GND
45	O	–	SD1_TXD2_P	46	I	–	SD1_RXD2_P
47	O	–	SD1_TXD2_N	48	I	–	SD1_RXD2_N
49	–	0	GND	50	–	0	GND
51	O	–	SD1_TXD3_P	52	I	–	SD1_RXD3_P
53	O	–	SD1_TXD3_N	54	I	–	SD1_RXD3_N
55	–	0	GND	56	–	0	GND
57	I	2.5	GE1_GTX_CLK	58	I	2.5	GE1_RX_CLK
59	O	2.5	GE1_TX_CLK	60	I	2.5	GE1_RX_CTL

Table 25. High-Speed Connector Pin Definition (continued)

MSC8156				HSC			
Pin No.	IO	V	Signal Name	Pin No.	IO	V	Signal Name
61	O	2.5	GE1_TX_CTL	62	I	2.5	GE1_RXD0
63	O	2.5	GE1_TXD0	64	I	2.5	GE1_RXD1
65	O	2.5	GE1_TXD1	66	I	2.5	GE1_RXD2
67	O	2.5	GE1_TXD2	68	I	2.5	GE1_RXD3
69	O	2.5	GE1_TXD3	70	I	0	GND
71	–	0	GND	72	I	2.5	GE2_GTX_CLK
73	I	2.5	GE2_RX_CLK	74	O	2.5	GE2_TX_CLK
75	O	2.5	GE2_RX_CTL	76	O	2.5	GE2_TX_CTL
77	O	2.5	GE2_RXD0	78	O	2.5	GE2_TXD0
79	O	2.5	GE2_RXD1	80	O	2.5	GE2_TXD1
81	O	2.5	GE2_RXD2	82	O	2.5	GE2_TXD2
83	O	2.5	GE2_RXD3	84	O	2.5	GE2_TXD3
85	B	–	nc	86	–	0	GND
87	B	–	nc	88	B	2.5	UART_TXD_GPIO29
89	B	2.5	EE0	90	B	2.5	UART_RXD_GPIO28
91	B	2.5	TMS	92	B	2.5	PORST_B
93	B	2.5	TRST_B	94	B	2.5	HRST_B
95	B	2.5	TCK	96	B	2.5	RCW_SRIO0_GPIO27_TMR4
97	B	2.5	TDI	98	B	2.5	RCW_SRIO1_GPIO25_TMR2
99	B	2.5	TDO	100	B	2.5	RCW_SRIO2_GPIO24_TMR1
101	B	2.5	I ² C	102	B	2.5	STOP_BS
103	B	2.5	I ² C	104	B	2.5	GPIO0_IRQ0
105	B	2.5	INT_OUT_B	106	B	2.5	GPIO1_IRQ1
107	B	2.5	NMI_B	108	B	2.5	SPI_SL_B_GPIO20
109	B	–	nc	110	B	2.5	SPI_MISO_GPIO19
111	O	2.5	BRD_ID0	112	B	2.5	SPI_MOSI_GPIO18
113	O	2.5	BRD_ID1	114	B	2.5	SPI_SCK_GPIO17
115	O	2.5	BRD_ID2	116	–	–	nc
117	–	5	nc	118	–	–	nc
119	B	2.5	DDR3_RST_B	120	–	–	nc
121	–	1	VCORE	122	2.5	–	VIO_2V5

Table 25. High-Speed Connector Pin Definition (continued)

MSC8156				HSC			
Pin No.	IO	V	Signal Name	Pin No.	IO	V	Signal Name
123	–	1	VCORE	124	2.5	–	VIO_2V5
125	–	1	VCORE	126	2.5	–	VIO_2V5
127	–	1	VCORE	128	1.5	–	VDDR
129	–	1	VCORE	130	1.5	–	VDDR
131	–	1	VCORE	132	1.5	–	VDDR
133	–	1	VCORE	134	1.5	–	VDDR
135	–	1	VCORE	136	1.5	–	VDDR
137	–	1	VCORE	138	1.5	–	VDDR
139	–	1	VCORE	140	0.75	–	VTT
141	–	1	VCORE	142	0.75	–	VTT
143	–	1	VCORE	144	0.75	–	VTT
145	–	1	VCORE	146	1	–	VSERDES
147	–	1	VCORE	148	1	–	VSERDES
149	–	1	VCORE	150	1	–	VSERDES

3.12.1 Mezzanine Identification

Three signals, BRD_ID[2:0], are used to identify the mezzanine when located on the AMC base card. These three signals are connected to ground through 0Ω resistors with BRD_ID0's pull down set to DNP. The pull ups on the base card sets the MSC8156 mezzanine tile to b001.

3.13 Mechanicals

3.13.1 Thermal Requirements

A heat sink is used to cool the MSC8156. The heat sink definition is based on thermal simulation within an ATCA/MicroTCA chassis with an air flow of >2 m/s.

3.13.2 Mezzanine Size and Component Envelope

The mezzanine is $70\text{mm} \times 39\text{mm}$, and when fitted on the AMC base card, the combined component layout complies with the “Full Size Mode Dimensions” of the AMC specification. Three mezzanines can be fitted onto the AMC base card.

Figure 6 shows the mezzanine layout.

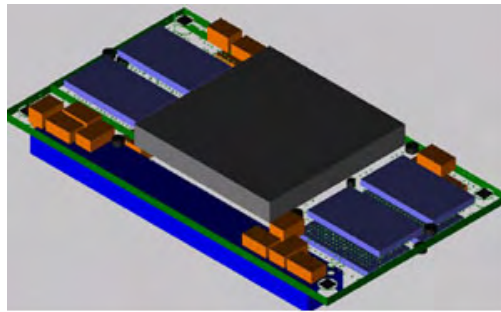


Figure 6. MSC8156 Mezzanine Layout

4 Revision History

Table 26. Document Revision History

Revision Number	Date	Substantive Change(s)
0	01/2010	Initial release.

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