

# DSC RTCESL 4.5.1 Release Notes

## 1 Overview

These release notes are for the DSP56800EX  
Real-Time Control Embedded Software  
Libraries release 4.5.1.

The purpose of this release is to recompile the  
whole library without the SLLD (64-bit data  
types support) attribute and the Bit Accurate  
Models (BAM) of RTCESL functions are added.

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## 2 What is new

All libraries are rebuilt without the SLLD attribute to avoid compilation warnings when RTCESL is a part of projects with the SLLD option. The inline functions can be compiled without the SLLD option if the SUPPORT\_64BIT\_DATA\_TYPE define is not defined.

The most important functions newly contain their Bit Accurate Models (BAM) for Matlab Simulink environment. Using the BAMs, you can simulate most motor-control applications. After a successful simulation, the Simulink schema can be transferred to the generated code using the Matlab Coder toolbox and the application can be executed from a target board. The DSC RTCESL 4.5.1 installer with the BAMs can be downloaded from the DOWNLOAD section at [www.nxp.com/rtesl](http://www.nxp.com/rtesl).

To create your simulation schema, open the BAM (.mdl file from the installation folder; for example c:\nxp\RTCESL\DSC\_bam; MATLAB 2020a or higher version is required). Connect the block inputs, outputs, and assigned block parameters (if any) and run the simulation.

If you want to transfer your Simulink schemas to the target board, download the model-based design toolbox at: [www.nxp.com/mbdt](http://www.nxp.com/mbdt).

## 3 Description

This release of RTCESL supports the following platforms:

- DSP56800EX

It contains the following libraries:

- MLIB
- GFLIB
- GDFLIB
- GMCLIB
- AMCLIB
- PCLIB

It is compiled on:

- CodeWarrior 11.1 (build 181224)

Optimization used:

- The maximum speed optimization is used for all libraries.

Memory models used:

- SDM - Small Data Model and Large Program Model. To achieve such configuration, uncheck all Large Data Memory Model and Huge Program Model items and check the Large Program Model item in the CodeWarrior Properties window.

- **LDM - Large Data and Large Program Model.** To achieve such configuration, uncheck all Small Data Memory Model and Huge Program Model Items and check the Large Data Model and Large Program Model items in the CodeWarrior Properties window.

The selected algorithms support the 16-bit and 32-bit fixed-point types only.

**This is the list of algorithms contained in this release:**

AMCLIB_ACIMCtrlMTPAInit_F16	GFLIB_DRampInit_F32
AMCLIB_ACIMCtrlMTPA_F16	GFLIB_DRamp_F16
AMCLIB_ACIMRotFluxObsrvInit_F16	GFLIB_DRamp_F32
AMCLIB_ACIMRotFluxObsrv_F16	GFLIB_FlexRampCalcIncr_F16
AMCLIB_ACIMSpeedMRASInit_F16	GFLIB_FlexRampInit_F16
AMCLIB_ACIMSpeedMRAS_F16	GFLIB_FlexRamp_F16
AMCLIB_AngleTrackObsrvInit_F16	GFLIB_FlexSRampCalcIncr_F16
AMCLIB_AngleTrackObsrv_F16	GFLIB_FlexSRampInit_F16
AMCLIB_CtrlFluxWkngInit_F16	GFLIB_FlexSRamp_F16
AMCLIB_CtrlFluxWkng_F16	GFLIB_Hyst_F16
AMCLIB_PMSMBemfObsrvABInit_F16	GFLIB_IntegratorInit_F16
AMCLIB_PMSMBemfObsrvAB_F16	GFLIB_Integrator_F16
AMCLIB_PMSMBemfObsrvDQInit_F16	GFLIB_Limit_F16
AMCLIB_PMSMBemfObsrvDQ_F16	GFLIB_Limit_F32
AMCLIB_TrackObsrvInit_F16	GFLIB_LowerLimit_F16
AMCLIB_TrackObsrv_F16	GFLIB_LowerLimit_F32
	GFLIB_Lut1D_F16
	GFLIB_Lut1D_F32
GDFLIB_FilterExpInit_F16	GFLIB_LutPer1D_F16
GDFLIB_FilterExp_F16	GFLIB_LutPer1D_F32
GDFLIB_FilterIIR1Init_F16	GFLIB_RampInit_F16
GDFLIB_FilterIIR1_F16	GFLIB_RampInit_F32
GDFLIB_FilterIIR2Init_F16	GFLIB_Ramp_F16
GDFLIB_FilterIIR2_F16	GFLIB_Ramp_F32
GDFLIB_FilterIIR3Init_F16	GFLIB_Sin_F16
GDFLIB_FilterIIR3_F16	GFLIB_Sqrt_F16
GDFLIB_FilterIIR4Init_F16	GMCLIB_Clark_F16
GDFLIB_FilterIIR4_F16	GMCLIB_DecouplingPMSM_F16
GDFLIB_FilterMAInit_F16	GMCLIB_ElimDcBusRipFOC_F16
GDFLIB_FilterMA_F16	GMCLIB_ElimDcBusRip_F16sas
	GMCLIB_ParkInv_F16
GFLIB_Acos_F16	GMCLIB_Park_F16
GFLIB_Asin_F16	GMCLIB_SvmDpwm_F16
GFLIB_AtanYX_F16	GMCLIB_SvmExDpwm_F16
GFLIB_Atan_F16	GMCLIB_SvmIct_F16
GFLIB_Cos_F16	GMCLIB_SvmStd_F16
GFLIB_CtrlBetaIPDpAWInit_F16	GMCLIB_SvmU0n_F16
GFLIB_CtrlBetaIPDpAW_F16	GMCLIB_SvmU7n_F16
GFLIB_CtrlBetaIPpAWInit_F16	
GFLIB_CtrlBetaIPpAW_F16	MLIB_AbsSat_F16
GFLIB_CtrlPIDpAWInit_F16	MLIB_AbsSat_F32
GFLIB_CtrlPIDpAW_F16	MLIB_Abs_F16
GFLIB_CtrlPIpAWInit_F16	MLIB_Abs_F32
GFLIB_CtrlPIpAW_F16	MLIB_Add4Sat_F16
GFLIB_DFlexRampCalcIncr_F16	MLIB_Add4Sat_F32
GFLIB_DFlexRampInit_F16	

MLIB_Add4_F16	MLIB_MacSat_F16
MLIB_Add4_F32	MLIB_MacSat_F32
MLIB_AddSat_F16	MLIB_MacSat_F32lss
MLIB_AddSat_F32	MLIB_Mac_A32ass
MLIB_Add_A32as	MLIB_Mac_F16
MLIB_Add_A32ss	MLIB_Mac_F32
MLIB_Add_F16	MLIB_Mac_F32lss
MLIB_Add_F32	MLIB_MnacRndSat_F16
MLIB_Clb_U16l	MLIB_MnacRndSat_F32
MLIB_Clb_U16s	MLIB_MnacRndSat_F32lls
MLIB_Conv_F16l	MLIB_MnacRnd_A32ass
MLIB_Conv_F32s	MLIB_MnacRnd_F16
MLIB_Div1QSat_A32as	MLIB_MnacRnd_F32
MLIB_Div1QSat_F16	MLIB_MnacRnd_F32lls
MLIB_Div1QSat_F16ll	MLIB_MnacSat_F16
MLIB_Div1QSat_F16ls	MLIB_MnacSat_F32
MLIB_Div1QSat_F32	MLIB_MnacSat_F32lss
MLIB_Div1QSat_F32ls	MLIB_Mnac_A32ass
MLIB_Div1Q_A32as	MLIB_Mnac_F16
MLIB_Div1Q_A32ll	MLIB_Mnac_F32
MLIB_Div1Q_A32ls	MLIB_Mnac_F32lss
MLIB_Div1Q_A32ss	MLIB_Msu4RndSat_F16
MLIB_Div1Q_F16	MLIB_Msu4RndSat_F32
MLIB_Div1Q_F16ll	MLIB_Msu4Rnd_F16
MLIB_Div1Q_F16ls	MLIB_Msu4Rnd_F32
MLIB_Div1Q_F32	MLIB_Msu4Sat_F32ssss
MLIB_Div1Q_F32ls	MLIB_Msu4_F32ssss
MLIB_DivSat_A32as	MLIB_MsuRndSat_F16
MLIB_DivSat_F16	MLIB_MsuRndSat_F32
MLIB_DivSat_F16ll	MLIB_MsuRndSat_F32lls
MLIB_DivSat_F16ls	MLIB_MsuRnd_A32ass
MLIB_DivSat_F32	MLIB_MsuRnd_F16
MLIB_DivSat_F32ls	MLIB_MsuRnd_F32
MLIB_Div_A32as	MLIB_MsuRnd_F32lls
MLIB_Div_A32ll	MLIB_MsuSat_F16
MLIB_Div_A32ls	MLIB_MsuSat_F32
MLIB_Div_A32ss	MLIB_MsuSat_F32lss
MLIB_Div_F16	MLIB_Msu_A32ass
MLIB_Div_F16ll	MLIB_Msu_F16
MLIB_Div_F16ls	MLIB_Msu_F32
MLIB_Div_F32	MLIB_Msu_F32lss
MLIB_Div_F32ls	MLIB_MulNegRndSat_A32
MLIB_Log2_U16	MLIB_MulNegRndSat_F16as
MLIB_Mac4RndSat_F16	MLIB_MulNegRnd_A32
MLIB_Mac4RndSat_F32	MLIB_MulNegRnd_F16
MLIB_Mac4Rnd_F16	MLIB_MulNegRnd_F16as
MLIB_Mac4Rnd_F32	MLIB_MulNegRnd_F32
MLIB_Mac4Sat_F32ssss	MLIB_MulNegRnd_F32ls
MLIB_Mac4_F32ssss	MLIB_MulNegSat_A32
MLIB_MacRndSat_F16	MLIB_MulNegSat_F16as
MLIB_MacRndSat_F32	MLIB_MulNeg_A32
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MLIB_MacRnd_A32ass	MLIB_MulNeg_F16as
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MLIB_MacRnd_F32	MLIB_MulNeg_F32ss
MLIB_MacRnd_F32lls	MLIB_MulRndSat_A32

MLIB\_MulRndSat\_F16  
MLIB\_MulRndSat\_F16as  
MLIB\_MulRndSat\_F32  
MLIB\_MulRndSat\_F32ls  
MLIB\_MulRnd\_A32  
MLIB\_MulRnd\_F16  
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MLIB\_Mul\_F32ss  
MLIB\_NegSat\_F16  
MLIB\_NegSat\_F32  
MLIB\_Neg\_F16  
MLIB\_Neg\_F32  
MLIB\_Rcp1Q1\_A32s  
MLIB\_Rcp1Q\_A32s  
MLIB\_Rcp1\_A32s  
MLIB\_Rcp\_A32s  
MLIB\_RndSat\_F16l  
MLIB\_Rnd\_F16l  
MLIB\_Sat\_F16a  
MLIB\_Sh1LSat\_F16  
MLIB\_Sh1LSat\_F32  
MLIB\_Sh1L\_F16  
MLIB\_Sh1L\_F32  
MLIB\_Sh1R\_F16  
MLIB\_Sh1R\_F32  
MLIB\_ShLBiSat\_F16

MLIB\_ShLBiSat\_F32  
MLIB\_ShLBi\_F16  
MLIB\_ShLBi\_F32  
MLIB\_ShLSat\_F16  
MLIB\_ShLSat\_F32  
MLIB\_ShL\_F16  
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MLIB\_ShRBiSat\_F16  
MLIB\_ShRBiSat\_F32  
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MLIB\_ShR\_F16  
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MLIB\_Sign\_F16  
MLIB\_Sign\_F32  
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MLIB\_Sub4Sat\_F32  
MLIB\_Sub4\_F16  
MLIB\_Sub4\_F32  
MLIB\_SubSat\_F16  
MLIB\_SubSat\_F32  
MLIB\_Sub\_A32as  
MLIB\_Sub\_A32ss  
MLIB\_Sub\_F16  
MLIB\_Sub\_F32  
  
PCLIB\_Ctrl2P2ZInit\_F16  
PCLIB\_Ctrl2P2Z\_F16  
PCLIB\_Ctrl3P3ZInit\_F16  
PCLIB\_Ctrl3P3Z\_F16  
PCLIB\_CtrlPIDInit\_F16  
PCLIB\_CtrlPID\_F16  
PCLIB\_CtrlPIInit\_F16  
PCLIB\_CtrlPI\_F16  
PCLIB\_CtrlPIandLPInit\_F16  
PCLIB\_CtrlPIandLP\_F16

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