UM10431

GreenChip TEA1795T synchronous rectifier controller demo board

Rev. 1 — 26 October 2010 **User manual**

Document information

Info	Content
Keywords	TEA1795T, LLC converter, resonant converter, dual Synchronous Rectifier (SR) driver, power supply, demo board.
Abstract	This user manual describes how the TEA1795T demo board can be used in a resonant converter. In addition to the TEA1795T, the demo board contains two power MOSFETs and output capacitors. There are two versions of the demo board available: 6 A, 30 V and 20 A, 12 V. The demo board replaces the secondary part of the resonant converter, excluding the feedback hardware

Revision history

Rev	Date	Description
1.0	20101026	First issue

Contact information

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1. Introduction

This document describes the TEA1795T demo board. A functional description is provided, supported by a set of measurements illustrating the performance of the TEA1795T. The demo board contains the secondary part of a single output LLC converter, excluding the control hardware. To use the demo board correctly, an LLC converter board in which the secondary part can be replaced by the demo board is required. Furthermore, two sense wires need to be connected to the control hardware to provide the feedback loop for controlling the output voltage.

2. The TEA1795T

The TEA1795T is a dual Synchronous Rectifier (SR) driver IC (or SR driver) for resonant converters. It can easily drive MOSFETs used to replace the rectifier diodes on the secondary side.

A simple control algorithm built into the IC determines when a MOSFET needs to be turned on or off: at V_{DS} = −220 mV the MOSFET is turned on; between −25 mV and −12 mV the IC will be in Regulation mode; above −12 mV the MOSFET will be turned off. In Regulation mode, the drain-source voltage is held constant at −25 mV to minimize turn-off time.

A simplified state diagram of the TEA1795T is shown in Figure 1. The −25 mV level was built in to minimize the turn-off delay time (at the expense of additional dissipation). In addition, two blanking time periods were added to prevent spurious switching after a MOSFET is turned on or off.

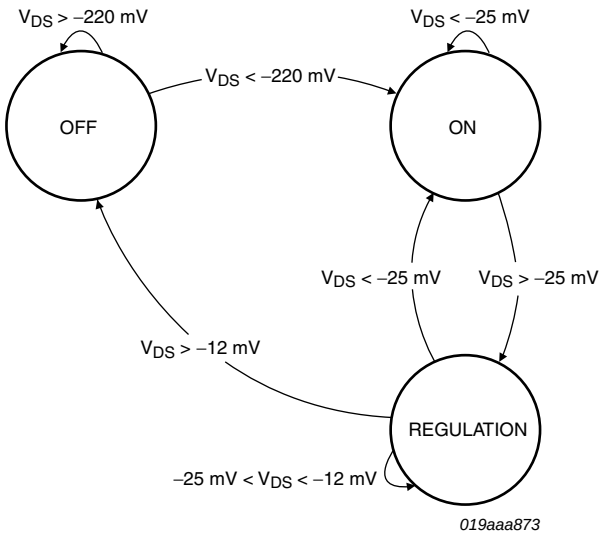


Fig 1. Simplified state diagram of the TEA1795T

To measure the drain-source voltage of the MOSFETs, sense pins DSA and SSA are connected, respectively, to the drain and source of MOSFET A. Sense pins DSB and SSB are connected to MOSFET B. In addition to the voltage drop due to R_{DSon} of the

MOSFETs, voltage drops are present across the tracks and the package. Incorporating two separate sense pins (SSA and SSB) helps to minimize the influence of these voltage drops.

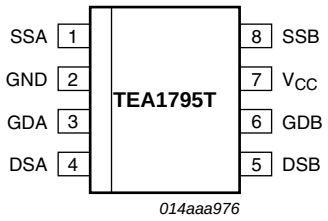


Fig 2. Pin configuration

3. Demo board setup

To ensure the demo board can be used in a variety of applications, two versions are available: TEA1795T demo board v1 contains two NXP Semiconductors PSMN025-100D (100 V 25 mΩ DPAK) power MOSFETS and is intended for high-voltage, low-current applications (e.g as a notebook adaptor). TEA1795T demo board v2 contains two NXP Semiconductors PSMN4R5-40PS (40 V 4.5 mΩ TO220) power MOSFETS and was designed for low-voltage, high-current applications (e.g. in a desktop PC power supply). Because of the small heat sink included in the TEA1795T demo board v2, a fan should be used for forced cooling.

Remark: The heat sinks are connected to the MOSFET drains in both versions of the demo board. It is possible to modify the TEA1795T demo board v2 to connect the heat sink to ground.

The demo boards were designed to be incorporated into an existing resonant power supply, by replacing the secondary circuit. The demo board is connected to the secondary side of the transformer.

Note that when replacing a diode in the high-voltage line of the transformer with a MOSFET located in the ground path, the center tap of the transformer must be disconnected from ground and connected to V_{out} (see Figure 3). Note also that no provisions have been made to provide a feedback loop to control the output voltage of the demo board. Therefore, connections are needed between the two PCBs to close the loop (see Figure 4). The points on the demo board where the secondary side of the transformer, the feedback loop and the output wires should be connected are illustrated in Figure 5.

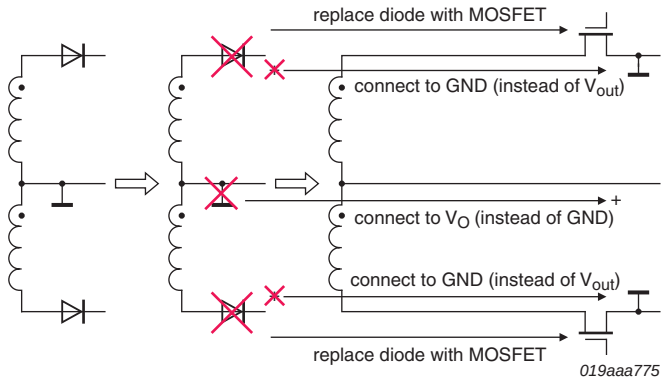


Fig 3. Connecting the transformer to the demo board

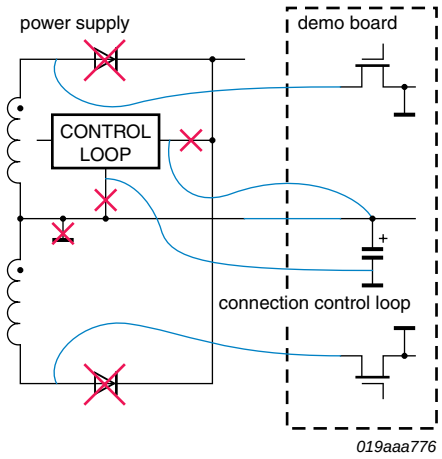


Fig 4. Connecting the control loop to the demo board

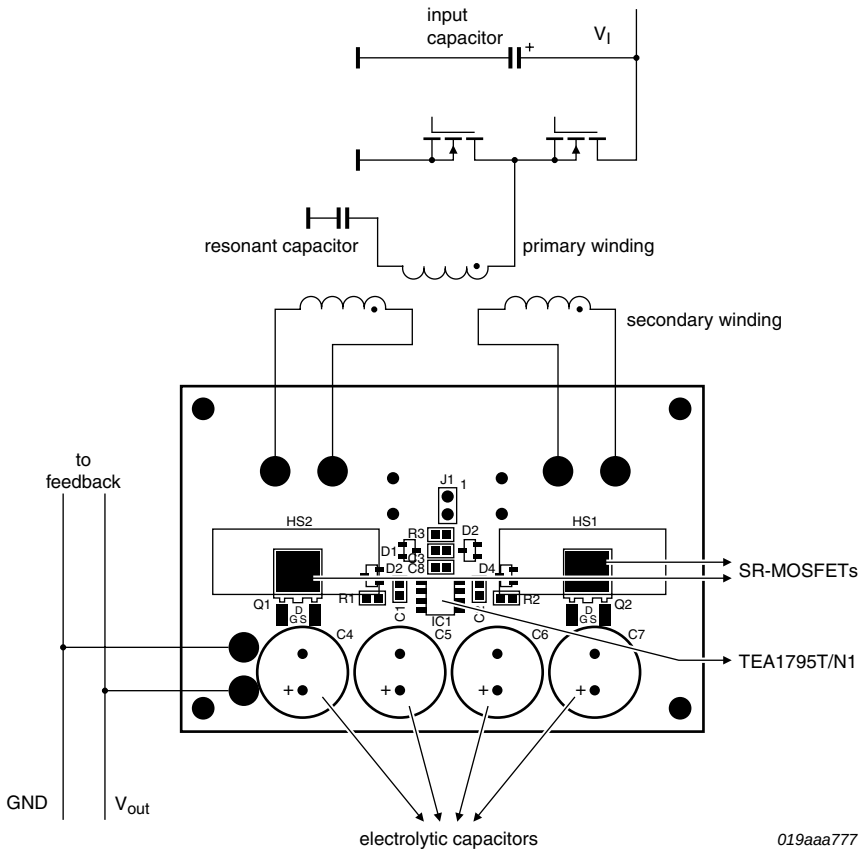
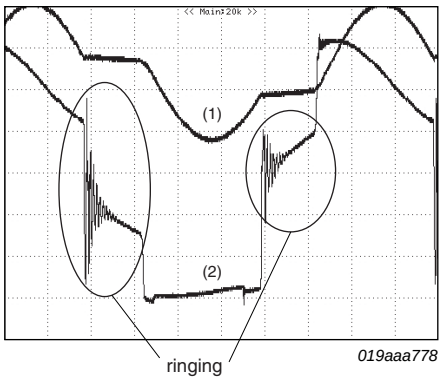


Fig 5. Placement of demo board in existing resonant converter

Low-pass filters (R1 & C1 and R2 & C2) are used to filter out ringing in the drain-source voltage caused by the part of the secondary winding that is not coupled to the main secondary winding and the drain-source capacitance. This filtering is needed to prevent the MOSFETs being turned on by mistake. A plot of the ringing in the drain-source voltage is shown in Figure 6. Ringing occurs when one of the MOSFETs stops conducting current or when the half-bridge voltage is changing (rising/falling).



(1) Transformer primary current.

(2) V_{DS}.

Fig 6. Drain-source ringing caused by MOSFET switching (without filtering)

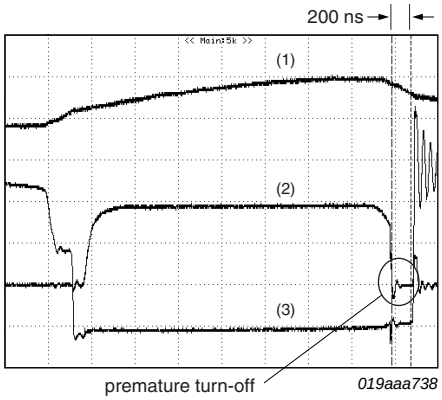
As discussed in application note AN10954, measurement of the drain-source voltage includes voltage drops across the tracks, bonding wires, and the pins of the package. These voltages drops are due, in part, to parasitic inductance, which can lead to serious measurement errors. The RC filters provided on the demo boards to filter out drain-source ringing can also be used to compensate for parasitic inductance. The influence of the parasitic inductance can be minimized by satisfying the following equation:

$$\frac{L_{par}}{R_{DSon}} = Rx \times Cx \quad (x = 1 \text{ or } 2) \tag{1}$$

The magnitude of the parasitic inductance depends on the package used and is much higher in a TO220 package than in a DPAK package. Drain-source ringing is more of an issue with a DPAK package. The dimensioning of the filters in the demo boards takes account of this. RC filter tuning on the TEA1795T demo board v1 is biased towards filtering drain-source ringing whereas the filters on the TEA1795T demo board v2 are optimized to reduce parasitic inductance.

With the TEA1795T demo board v2, the mode of operation of the converter needs to be taken into account. The dimensions of the compensation filter were calculated for Discontinuous Current Mode (DCM). The filter has not been optimized for Continuous Current Mode (CCM), and will need to be adjusted since parasitic inductance has less influence at the instant the MOSFET is turned off. The plot in Figure 7 was measured with the converter in CCM mode, C1 = 0 pF and I_{load} = 10 A.

Parasitic inductance causes the MOSFETs to turn off too early (premature turn-off). It is clear from Figure 7 and Figure 8 that the influence of parasitic inductance is much greater in DCM mode (1.2 μs) than in CCM mode (200 ns).



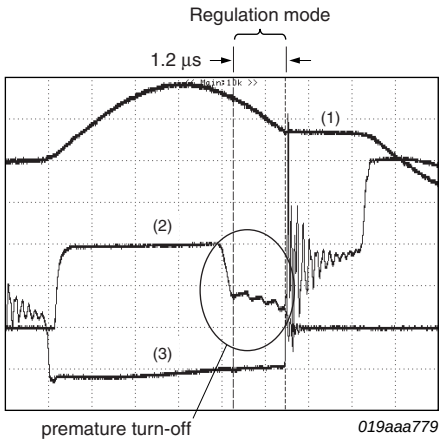
Rx = 3.9 kΩ; Cx = 0 pF; I_{load} = 10 A

(1) Transformer primary current.

(2) V_{GS}.

(3) V_{DS}.

Fig 7. CCM mode: small internal filter



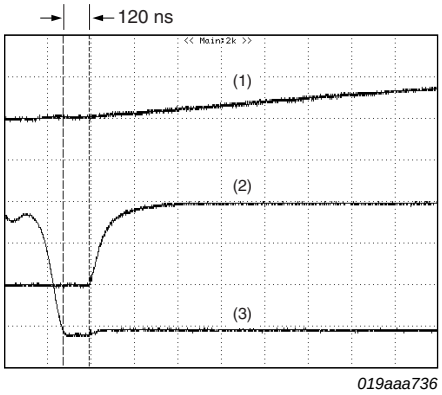
a. Parasitic inductance causes the IC to switch to Regulation mode 1.2 µs before the secondary current reaches 0 V.

Rx = 3.9 kΩ; Cx = 0 pF; I_{load} = 10 A

(1) Transformer primary current.

(2) V_{GS}.

(3) V_{DS}.



b. 120 ns turn-on delay time without external filter

Rx = 3.9 kΩ; Cx = 0 pF; I_{load} = 10 A

(1) Transformer primary current.

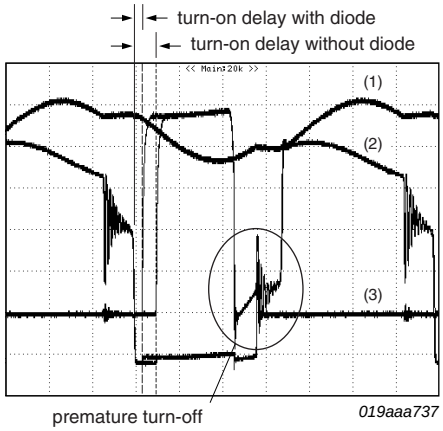
(2) V_{GS}.

(3) V_{DS}.

Fig 8. DCM mode: small internal filter

When the filter design is determined primarily by the value of the parasitic inductance (TO220 package), the voltage on the capacitor is clamped by a MOSFET or by an RF-diode with a low voltage drop to avoid a lengthy discharge time.

Adding an external filter reduces the premature turn-off time but increases the turn-on delay time. Ideally, the turn-on delay and premature turn-off times should be equal. The increase in the turn-on delay time can be limited by adding a clamping diode over Cx (see Figure 9).



Rx = 3.9 kΩ; Cx = 68 pF; I_{load} = 10 A

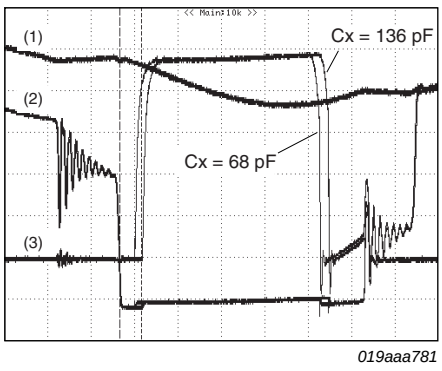
(1) Transformer primary current.

(2) V_{GS}.

(3) V_{DS}.

Fig 9. DCM mode: small external filter added

Increasing the size of the capacitor will increase the turn-on delay time and reduce the premature turn-off time (shifting the waveform to the right see; Figure 10).



Rx = 3.9 kΩ; I_{load} = 10 A

(1) Transformer primary current.

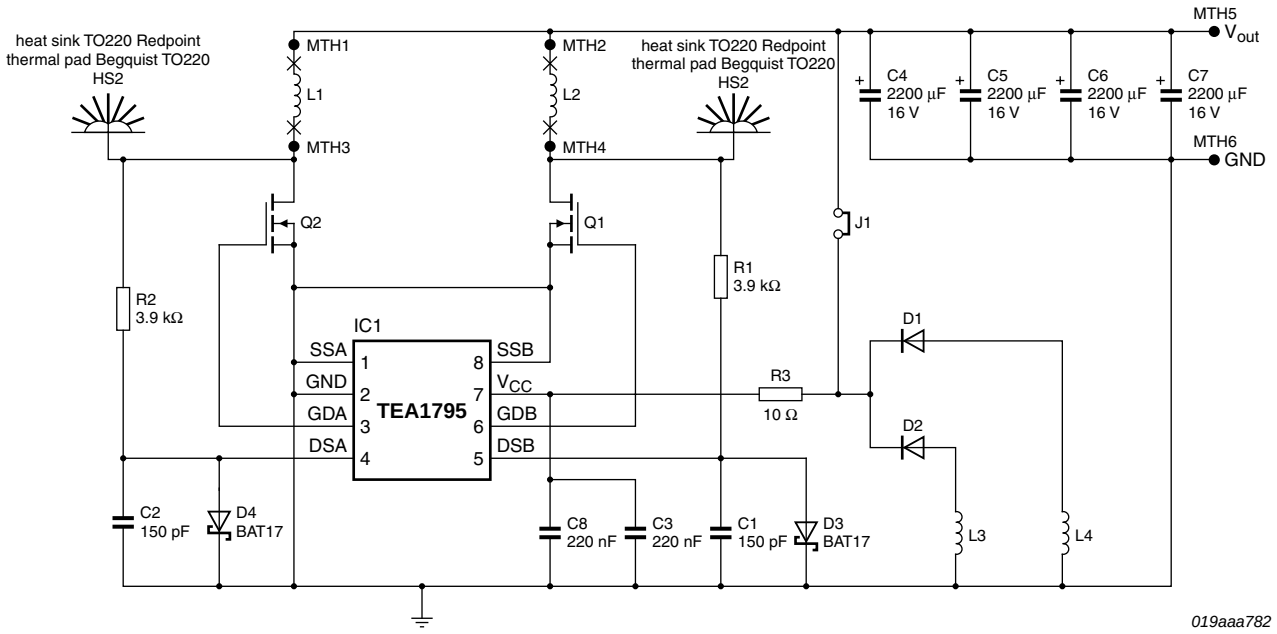
(2) V_{GS}.

(3) V_{DS}.

Fig 10. DCM mode: larger external filter

A 1 μA (max) current flows through pins DSA and DSB. Therefore, in order to ensure the voltage drop across the resistors does not exceed 4 mV, R1 = R2 = 3.9 kΩ.

A schematic of the TEA1795T demo board v2 is shown in Figure 11. The differences between the two demo boards are summarized in Table 1. The component placement is shown in Figure 12 and Figure 13.



The schematic of the TEA1795T demo board v1 is identical but with component values changed as indicated in Table 1.

Fig 11. Circuit diagram of the TEA1795T demo board v2

Table 1. Differences between demo boards

Component	TEA1795T demo board v1	TEA1795T demo board v2
C1	not mounted	150 pF/10 %/50 V/NPO
C2	not mounted	150 pF/10 %/50 V/NPO
C4	1000 µF/20 %/35 V; Rubycon ZL	2200 µF/20 %/16 V; Rubycon ZL
C5	1000 µF/20 %/35 V; Rubycon ZL	2200 µF/20 %/16 V; Rubycon ZL
C6	1000 µF/20 %/35 V; Rubycon ZL	2200 µF/20 %/16 V; Rubycon ZL
C7	1000 µF/20 %/35 V; Rubycon ZL	2200 µF/20 %/16 V; Rubycon ZL
D3	not mounted	BAT17
D4	not mounted	BAT17
HS1	heat sink FK-244-08-D-PAK; Fischer	heat sink TO220; Redpoint
HS2	heat sink FK-244-08-D-PAK; Fischer	heat sink TO220; Redpoint
Q1	PSMN025-100D; NXP Semiconductors	PSMN4R5-40PS; NXP Semiconductors
Q2	PSMN025-100D; NXP Semiconductors	PSMN4R5-40PS; NXP Semiconductors

[1] C1, C2, D3 and D4 are included in the schematic diagram (Figure 12) and PCB layout drawings (Figure 21 and Figure 22) but are not mounted on the TEA1795T demo board v1.

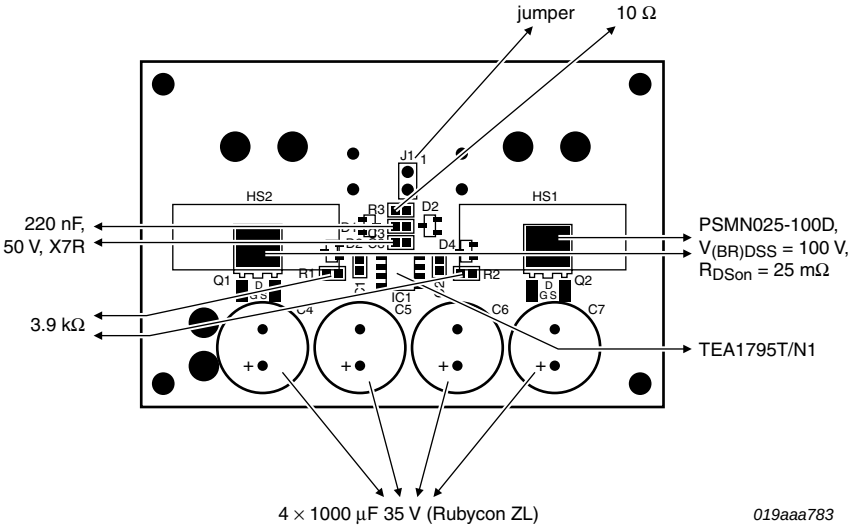


Fig 12. Component placement: TEA1795T demo board v1 (DPAK)

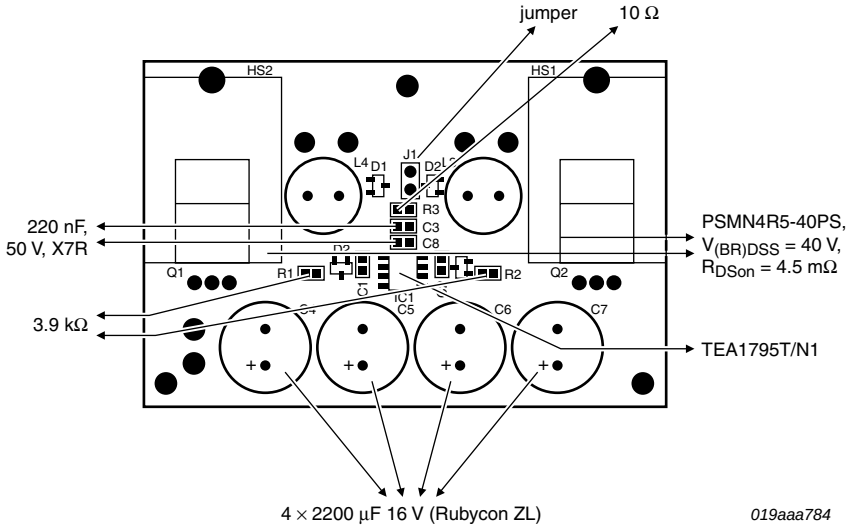


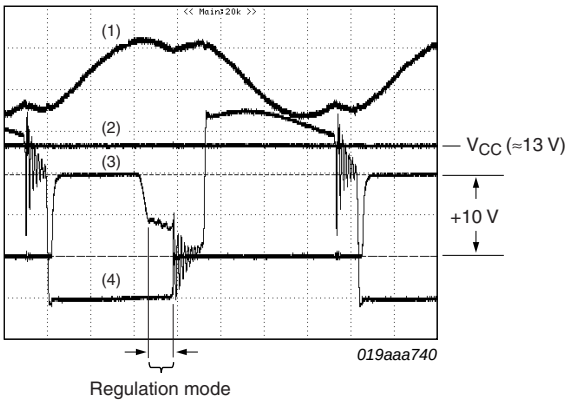
Fig 13. Component placement: TEA1795T demo board v2 (TO220)

4. Operation

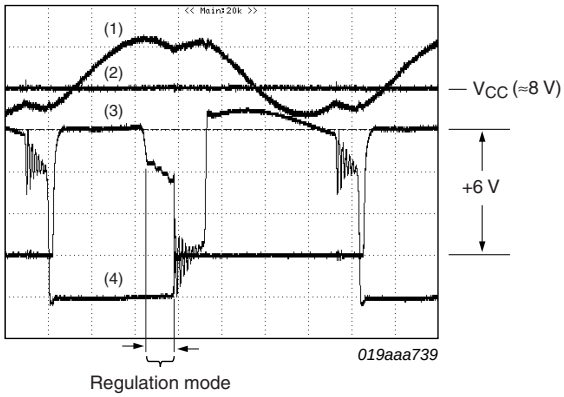
4.1 Turn-on and blanking time

The MOSFETs are turned on when the drain-source voltage falls below the turn-on threshold (−220 mV) and the gate is charged. An internal clamping circuit limits the maximum gate voltage to approximately 10 V (see Figure 14 (a)). The minimum gate voltage (V_{GS}) will be 6 V when V_{CC} is at a minimum (≈8 V).

A blanking time of 520 ns is built in to prevent the MOSFET turning off again immediately after turning on. After the blanking time, the gate voltage remains at the same level or is partly or totally discharged. In the plots in Figure 14, the gate remains charged. In the plot in Figure 15, the gate is discharged after the blanking time.



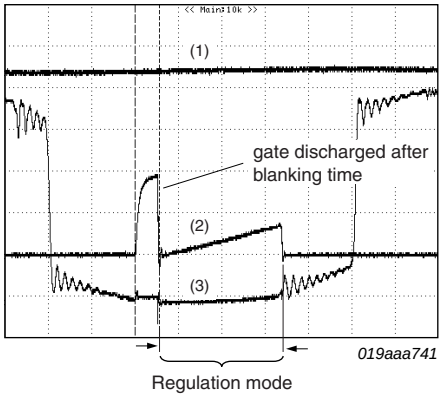
a. maximum gate voltage = 9.7 V



b. gate voltage = 6.1 V

(1) Primary current.
(2) V_{CC}.
(3) V_{GS}.
(4) V_{DS}.

Fig 14. Gate voltage



Gate voltage rises very slowly in Regulation mode because the charge current is limited to 5 mA.

(1) Primary current.

(2) V_{GS}.

(3) V_{DS}.

Fig 15. Blanking time after MOSFET turned on

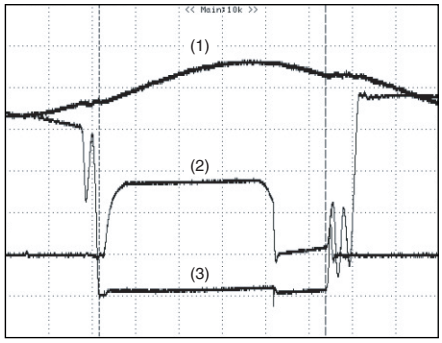
If V_{DS} rises above −25 mV, the gate will be discharged until V_{DS} is again equal to −25 mV and the IC remains in Regulation mode. The gate is discharged through an internal MOSFET (R_{DSon} = 24 Ω). A 5 mA current source provides the charge current, ensuring the gate voltage rises (see slowly rising edge in Figure 15).

4.2 Regulation mode and turn-off

Regulation mode is provided in order to minimize turn-off time. In this mode, the drain-source voltage is stabilized independently of the value of the current, at −25 mV (see Figure 8 and Figure 14). If the current falls so low that it's impossible to retain a drain-source voltage of −25 mV, the MOSFET will be turned off. In Regulation mode, the gate voltage is stabilized at just above the threshold voltage for turning off the MOSFET. Therefore, only a small fall in V_{DS} is needed to turn off the MOSFET.

4.3 Compromise between turn-on, turn-off and blanking times

In Figure 16 (a), a small filter (R1 = 3.9 kΩ and C1 = 0 pF) was added to reduce ringing. As can be seen, the turn-on behavior is close to ideal. However, the premature turn-off time is too long. The gate pulse can be shifted to the right by increasing the value of Cx (to 150 pF in this example; see Figure 16 (b)) and adding a clamping diode. This improves the turn-off behavior but results in a less ideal turn-on time.



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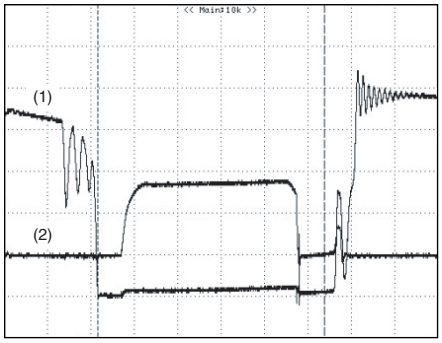
a. C1 = 0 pF

(1) Transformer primary current.
(2) V_{GS}.
(3) V_{DS}.



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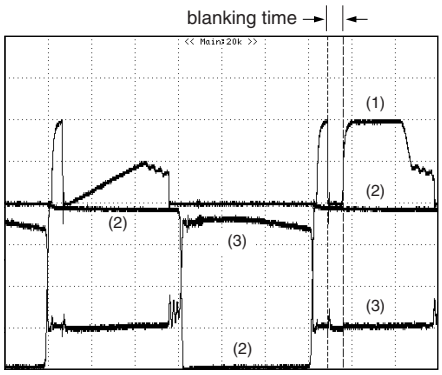
b. C1 = 150 pF; clamping diode added

(1) V_{DS}.
(2) V_{GS}.

Fig 16. Adjusting turn-on/turn-off behavior

The value of Cx should be selected such that the gate pulse is centered in relation to the MOSFET current. An additional blanking time has been built in to prevent spurious switching after the MOSFET has been turned off (see Figure 17).



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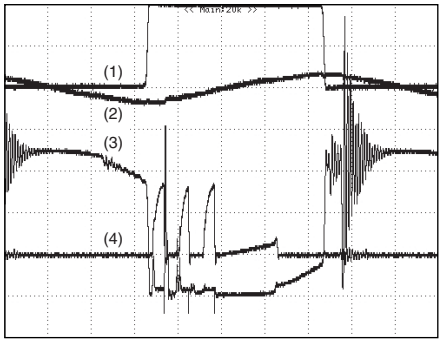
(1) V_{GS}.
(2) Half-bridge point.
(3) V_{DS}.

Fig 17. Blanking time after MOSFET turned off

When the blanking time has expired, it is possible to charge the gate and turn the MOSFET on again, so multiple pulses are possible (see Figure 18).



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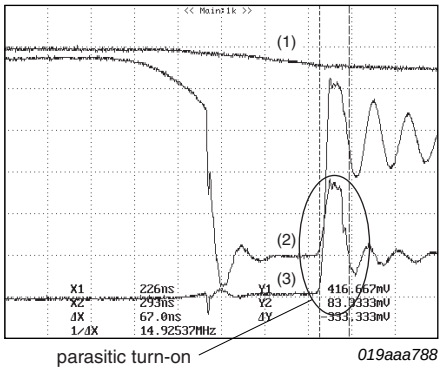
(1) Primary half-bridge voltage.
(2) Primary current.
(3) V_{DS}.
(4) V_{GS}.

Fig 18. Multiple turn-on pulses

4.4 Parasitic turn-on

When $V_{DS} > -12$ mV, an internal sink MOSFET is turned on. However, it might not start conducting immediately due to an internal delay in the IC, reducing sinking capability. During the rising edge on V_{GS}, the MOSFET will be turned on by the Miller capacitance of the MOSFET. This is illustrated in Figure 19.



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(1) Primary current.
(2) V_{GS}.
(3) V_{DS}.

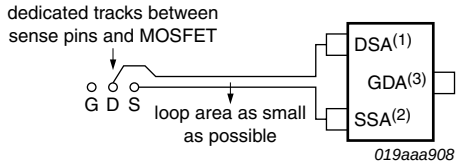
Fig 19. Parasitic turn-on due to rising edge on V_{DS}

5. PCB layout

5.1 Layout considerations

To ensure optimal performance and to minimize impedance, the following guidelines should be taken into account when designing the PCB layout:

- Dedicated tracks should be used to connect the sense pins on the IC to the MOSFET pins and the tracks should be as short as possible.
- The loop area between the drain sense track and the source sense track should be as small as possible.



(1) DSA = drain sense input (MOSFET A)

(2) SSA = source sense input (MOSFET A)

(3) GDA = gate driver output (MOSFET A)

Fig 20. Layout recommendations

5.2 Copper pattern

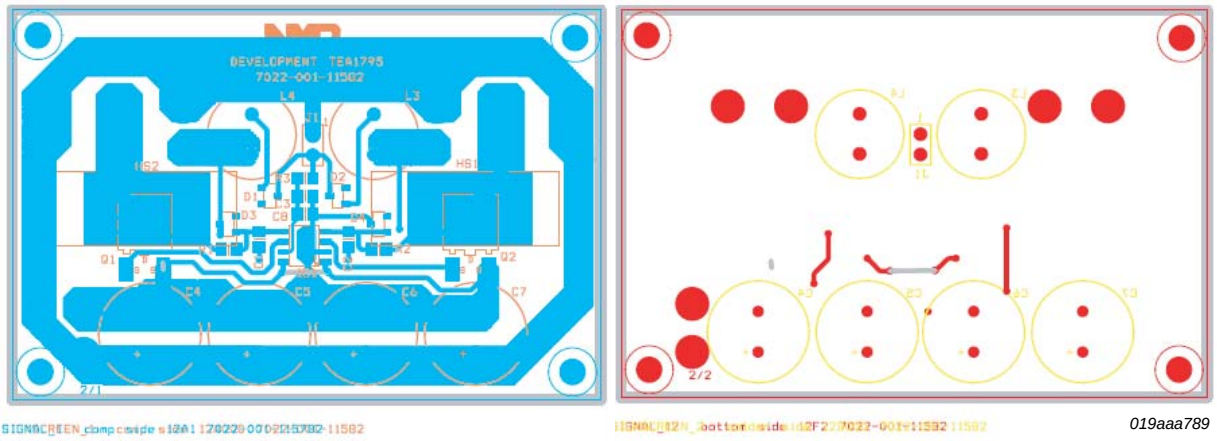


Fig 21. Layout of TEA1795T demo board v1 (DPAK)

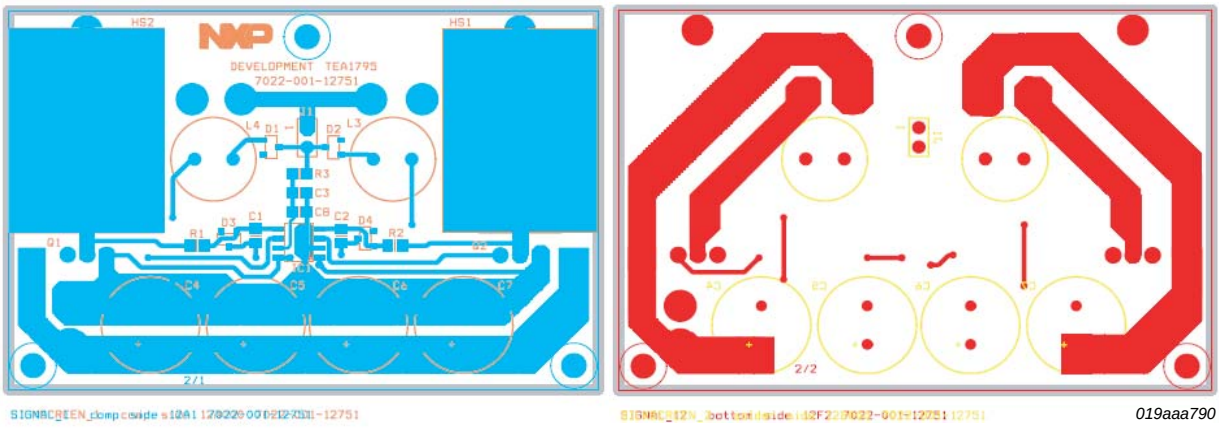


Fig 22. Layout of TEA1795T demo board v2 (TO220)

6. Bill of materials

Table 2. Bill of materials

Component	TEA1795T demo board v1	TEA1795T demo board v2
C1	not mounted	150 pF/10 %/50 V/NPO
C2	not mounted	150 pF/10 %/50 V/NPO
C3	220 nF/10 %/ 50 V (DC)	220 nF/10 %/50 V (DC)
C4	1000 μF/20 %/35 V; Rubycon ZL	2200 μF/20 %/16 V; Rubycon ZL
C5	1000 μF/20 %/35 V; Rubycon ZL	2200 μF/20 %/16 V; Rubycon ZL
C6	1000 μF/20 %/35 V; Rubycon ZL	2200 μF/20 %/16 V; Rubycon ZL
C7	1000 μF/20 %/35 V; Rubycon ZL	2200 μF/20 %/16 V; Rubycon ZL
C8	220 nF/10 %/50 V (DC) X7R	220 nF/10 %/50 V (DC) X7R
D1	not mounted	not mounted
D2	not mounted	not mounted
D3	not mounted	BAT17
D4	not mounted	BAT17
HS1	heat sink FK-244-08-D-PAK Fischer	heat sink TO220 Redpoint thermal pad Bergquist TO220
HS2	heat sink FK-244-08-D-PAK Fischer	heat sink TO220 Redpoint thermal pad Bergquist TO220
IC1	TEA1795T/N1	TEA1795T/N1
J1	micro shunt pitch 2.54 mm jumper or equivalent	micro shunt pitch 2.54 mm jumper or equivalent
L1	not mounted	not mounted
L2	not mounted	not mounted
L3	not mounted	not mounted
L4	not mounted	not mounted
Q1	PSMN025-100D; NXP Semiconductors	PSMN4R5-40PS; NXP Semiconductors
Q2	PSMN025-100D; NXP Semiconductors	PSMN4R5-40PS; NXP Semiconductors
R1	3.9 kΩ/1 %/0.1 W	3.9 kΩ/1 %/0.1 W
R2	3.9 kΩ/1 %/0.1 W	3.9 kΩ/1 %/0.1 W
R3	10 Ω/1 %/0.1 W	10 Ω/1 %/0.1 W

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8. Contents

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Date of release: 26 October 2010
Document identifier: UM10431