UM TFF11xxxHN

User Manual TFF11xxxHN evaluation board

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Document information

Info	Content
Keywords	TFF11xxxHN, LO generator, Ku-band, Satellite, VSAT, PLL, phase noise
Abstract	This document explains the TFF11XXX evaluation Board.

Revision history

Rev	Date	Description
0.1	2009 June 18	First Draft Release.
0.2	2009 June 26	Demo board schematic comp values corrected
0.3	2009 Jul 17	Final updates for first release
0.4	2009 Aug 3	Loop filter Optimization section extended
0.5	2009 Oct 16	Demo board schematic updated (LF comp. values) and loop filter optimization section added.
0.51	2010 May 18	Corrections added to jumper setting N
0.52	2010 Oct 15	Value decoupling capacitor pin 1to GND changed from 10nF to 1nF
0.53	2011 Feb. 11	Vreg_vco recommendation added, explanation PLL tool extended

Contact information

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1. Introduction

The TFF11XXXHN is a low phase noise, high frequency accuracy microwave (Ku band) local oscillator generator implemented in Silicon Germanium High Ft process. This device can be used in many applications such as telecommunication equipment, outdoor units for Satellite (VSAT) and other applications.

When a frequency doubler or sub-harmonic mixer is applied the frequency range can be extended to applications working up till 30Ghz.

The TFF11XXXHN evaluation board (EVB) is designed to evaluate the performance of the device for a fixed divider ratio; however this ratio can be changed by jumper settings. Consequently it might be needed to re-optimize the PLL loop-filter accordingly. Drawings of the board layout, bill of material, and some typical results are given.

Figure 1 shows the evaluation board.

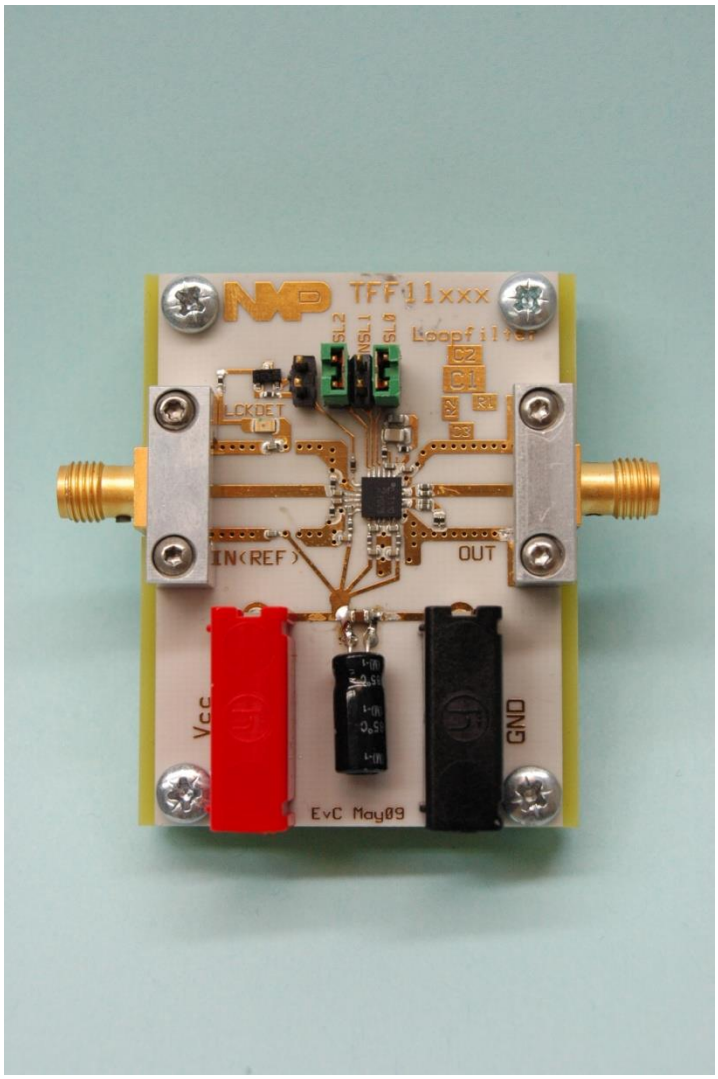

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Fig 1. Evaluation board

2. General description.

The TFF11XXXHN is a LO generator that consists of a VCO with output buffer, a programmable divider and a phase/frequency comparator with charge pump output and lock detector. With these blocks one can implement a Phased Locked Loop (PLL). By locking an integer fraction of the VCO frequency to a crystal reference frequency excellent frequency stability can be obtained compared to more traditional LO's implemented with Dielectric Resonator (DRO). By using a relatively wide loop bandwidth in the PLL the phase noise inside this loop bandwidth can be lowered. By using this method for satellite applications the phase noise performance can be brought to the IES-308 Intelsat requirements.

In Figure 2 the simplified internal circuit of the TFF11XXX is given.

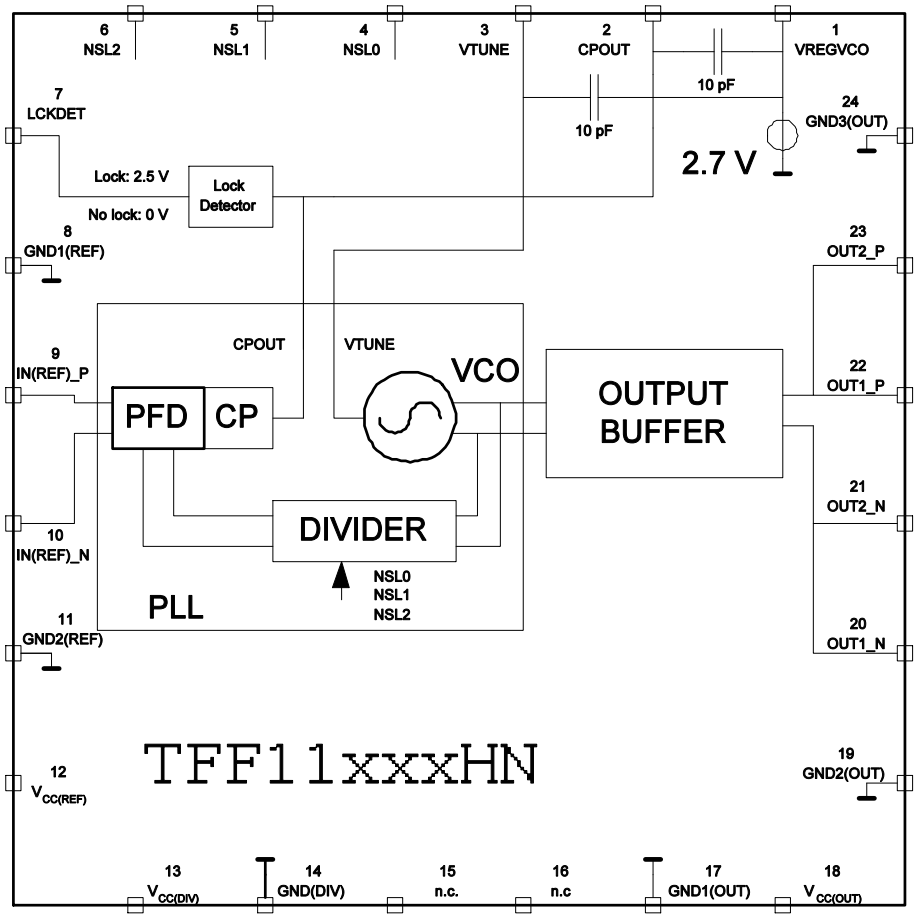

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Fig 2. TFF11xxx block diagram

Circuit description:
the VCO output signal is fed to a frequency divider, programmable by MSL0 to MSL2, and then compared to the reference frequency inside the Phase Frequency Discriminator (PFD), output of the PFD leads to a charge pump, and via an external loop-filter (required for loop stability and damping of the reference spurious) the "error-signal" is fed back to the VCO.

The VCO output signal is buffered before it routes to the IC outputs to avoid phase noise degradation by load impedance variations and to bring the impedance to required level.

The Reference input signal as well as the LO output signals are differential to enable common mode interference suppression.

3. Application Board

The TFF11XXX EVB simplifies the evaluation of the TFF11XXX functionality and performance. The EVB enables testing of the device performance and only requires an external reference. The board is connectorized with signal input and output SMA

3.1 Application Circuit

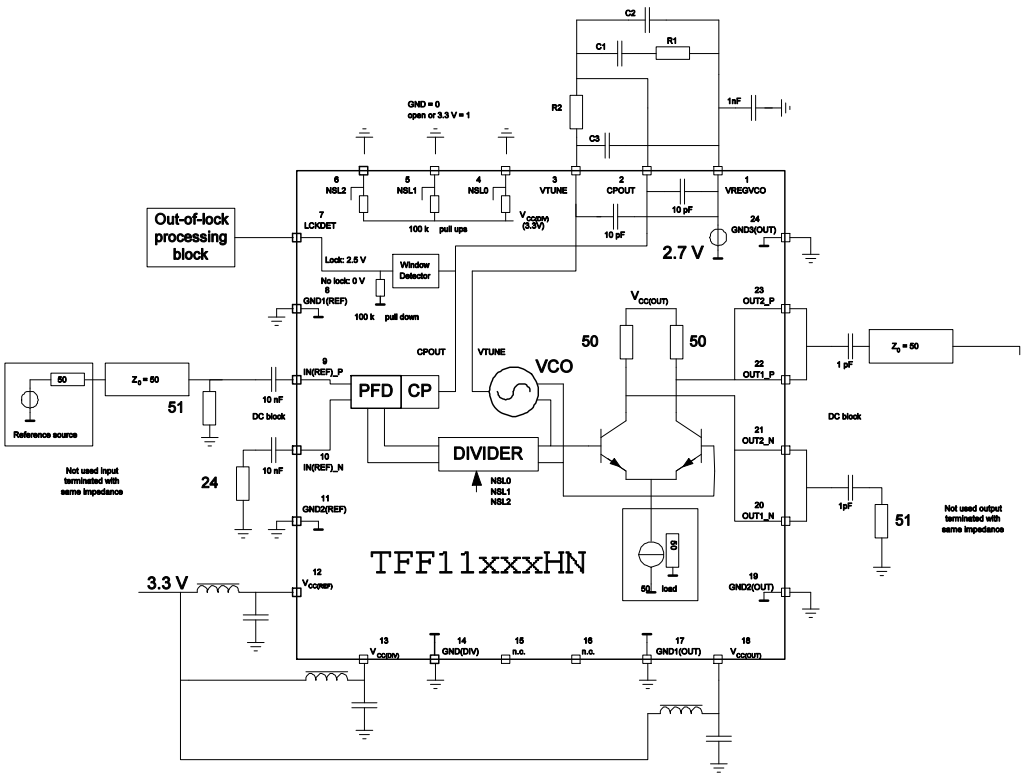

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Fig 3. Single ended typical application diagram

3.2 EVB schematics

Appendix 1 shows the evaluation board schematics.

3.3 Board Layout

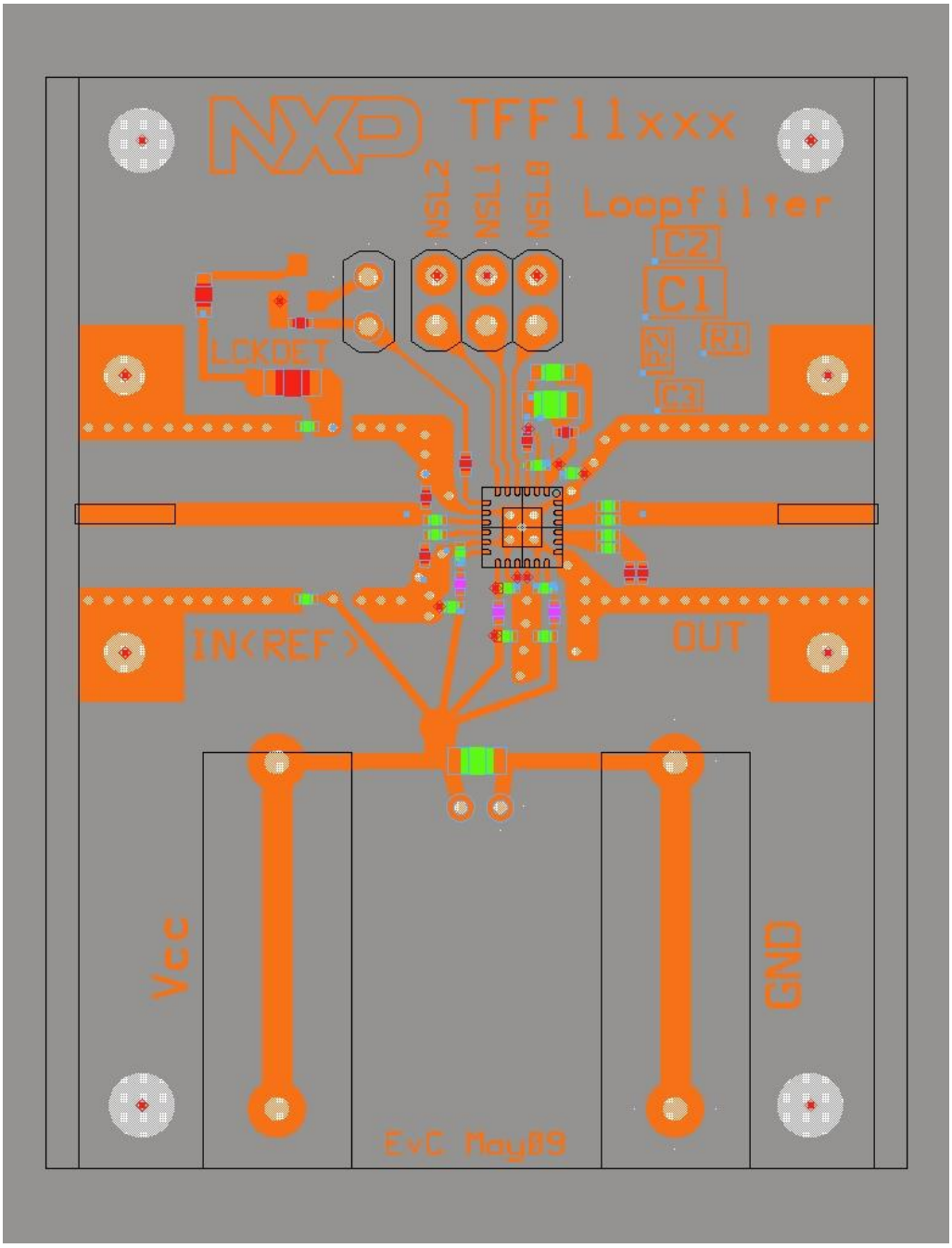

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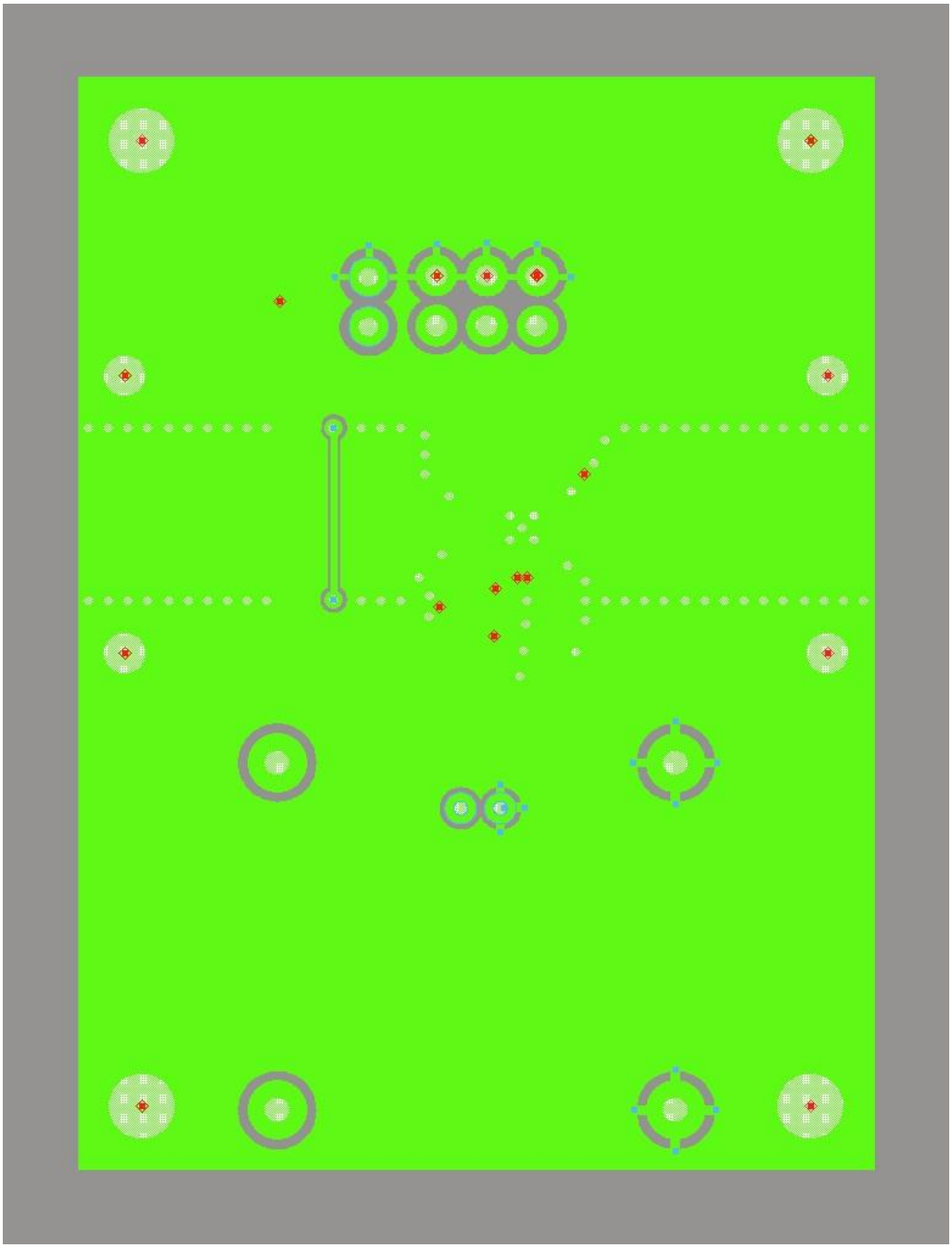
Fig 4. Board layout top side



(1)

Fig 5. Board layout bottom side

3.4 PCB layout hints/recommendations

A proper PCB layout is an essential part of an RF circuit design. The EVB of the TFF11XXX can serve as a guideline for laying out a board using the TFF11XXX however this board is not optimized for PCB area used. Use controlled impedance lines for all high frequency inputs and outputs. Bypass V_{CC} with decoupling capacitors, preferable located as close as possible to the device Vcc with short connection towards the corresponding GND pin as possible. For long bias lines it may be necessary to add decoupling capacitors along the line further away from the device. Proper grounding is assured by connecting the exposed die pad under the device with multiple via holes directly to the GND plane.
The material that has been used for the EVB is Rogers 4233, 0.5mm thickness two layer stack with the bottom layer fully dedicated as ground layer.

3.5 Bill of materials

See appendix 2 for the values/type numbers of used components.

4. Required Equipment for Evaluations

In order to measure the evaluation board the following is necessary.

- ✓ DC Power Supply op to 200 mA at 3.3 V
- ✓ A Signal generator capable of generating required reference signal for the PLL ranging from 50MHz till 816MHz (depending on divider setting in TFF11XXX) capable of delivering at least 0dBm output power.
- ✓ A RF spectrum analyzer or signal analyzer that covers the frequency range up till 14GHz or preferably higher in case spurious needs to be analyzed.
  ”Optional” a version with the capability of measuring phase noise is convenient.

Amp meter to measure the supply current (optional).

4.1 Connections and Set-up.

The TFF11XXX EVB is fully assembled and tested. Please follow the steps below for a step-by-step guide to operate the EVB and testing the device functions.

1. Connect the reference generator through the SMA connector at the left (please notice that for this demo board only unbalanced mode is possible)
2. Connect the signal analyzer (for example Spectrum Analyzer) at the right as shown in the picture below. Terminate the un-used RF output with a DC block and 50 Ohms termination since this output is DC coupled.
3. Connect the power supply (nominal 3.3Volts) to the board as shown below by the red/black DC cables/banana sockets.
4. Optionally connect for example the tuning voltage and/or locking status signal.

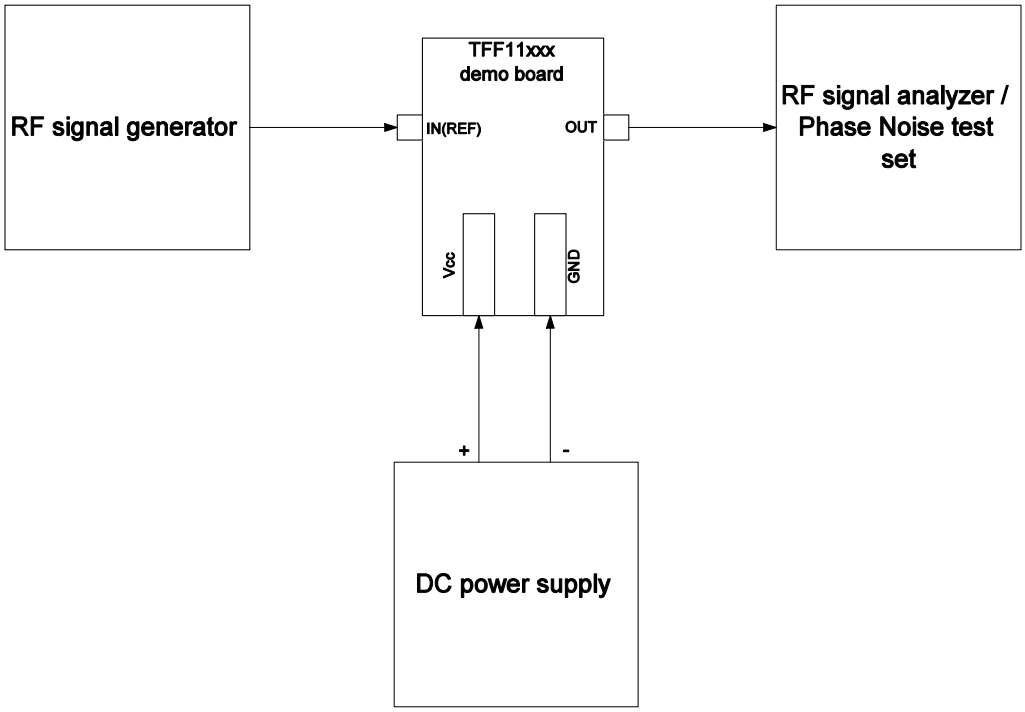


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Fig 6. Evaluation board in typical measurement set-up

4.2 Divider ratio settings

The TFF11XXX can generate a continuous wave (CW) signal in given frequency range by using a reference frequency in the range from 50MHz till 816MHz depending on used divider ratio setting. The divider ratio must be set by the jumpers NSL0,1 and 2. See figure 6 for jumper location and applied jumper settings. Please note that other possible settings are for test modes only.

Table 6. Divider setting as function of NSL2, NSL1 and NSL0

Setting number	NSL2	NSL1	NSL0	Divider value
0	0	0	0	16
1	0	0	1	32
2	0	1	0	64
3	0	1	1	128
4	1	0	0	256

(1)

Fig 7. Jumpers to set PLL divider ratio, 0=place jumper, 1=place no jumper

4.3 PLL Loop Filter Optimization

For each given output frequency and used divider ratio the PLL loop filter might be optimized for optimum phase noise and loop stability. In figure 8 the component positions for the loop filter are displayed.

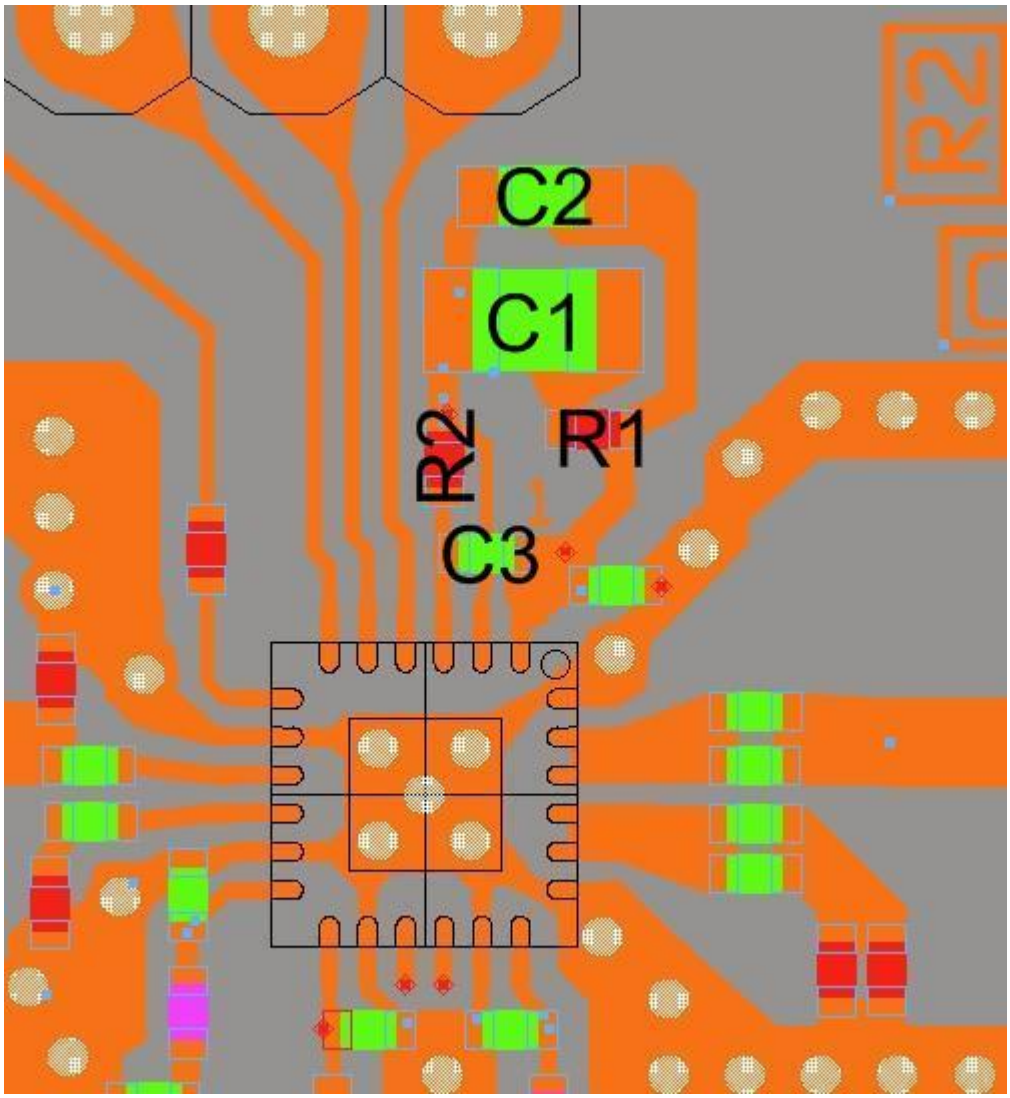


Fig 8. External loop filter components (C1, C2, C3, R1, R2) on EVB

In the table at the right top corner from appendix 1 the initial component values for the different divider ratio are given however depending on the application and its requirements those may require optimization.

4.3.1 Vreg_vco recommendation

This is a DC voltage stabilized inside the TFF1003 used to derive the VCO tuning voltage. An additional AC decoupling capacitor to GND may be applied (to suppress noise/AC ripple) but the capacitor value must not exceed 1nF. For larger capacitor values the internal stabilizer may become unstable at extreme conditions.

4.3.2 PLL Loop Filter considerations

To show the influence of the PLL loop filter BW some simulations were executed, depending on which parameter the design should be optimized one can choose for different PLL loop-filter BW.

Apart from spot noise, like phase noise at 100 kHz offset from carrier, other parameters that should be observed are:

- RMS phase jitter
- Reference spur suppression
- PLL phase margin (for stability)

Usually the RMS phase jitter gives a better representation for the system BER compared to spot noise.

For the double side band phase jitter simulation results (F=12.8GHz, N=64) are shown in figure 11. The integration interval for phase jitter ranges from 10 kHz till 10MHz.

One criterion that should not be forgotten is the control loop phase margin, which determines the stability of the loop. Depending on the loop filter BW peaking in the PN spectrum may occur.

4.4 PLL Loop filter optimization

For each given output frequency and used divider ratio the PLL loop filter might be optimized for optimum phase noise and loop stability.

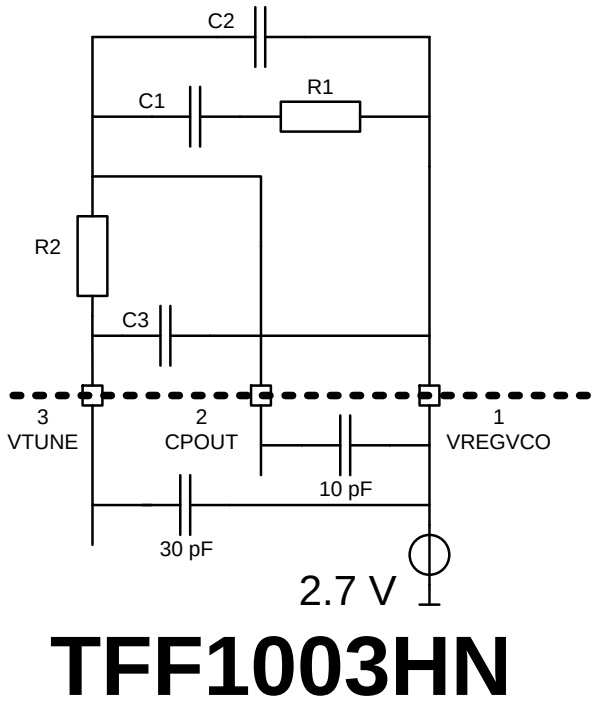


Figure 7 External loop filter components (C1, C2, C3, R1, R2) on EVB

Optimization can be focused on:

1) value for spot noise at given frequency offset
2) integrated RMS phase jitter in given frequency interval
3) loop stability/speed for example in case the reference frequency will be switched/modulated

The values given in the table below are start values for reasonable compromise, they may be optimized for each application by using a simulation tool.

Component	R1 (Ohms)	C1 (nF)	C2 (pF)	R2 (Ohms)	C3 (pF)
N=16	68	68	560	560	33
N=32	120	33	270	560	33
N=64	270	18	120	560	33
N=128	330	18	82	560	33
N=256	470	27	82	560	33

4.5 Explanation on simulation tool available from NXP

This tool can be used in general for each PLL, it calculates the loop BW, phase margin and plots the phase noise spectrum. Below some explanation in how to use the tool is given (partly copied from the tools “help function”.

4.5.1 Introduction

This applet is a fast and easy design tool for 3rd & 4th order Phase Locked Loops (PLL). It includes the following functions:

- Calculation of the loop filter for achieving a desired frequency response.
- Simulation of the PLL for a given user defined loop filter.
- Calculation of the noise performance of the PLL, including the contribution of the quantization noise for a fractional-N PLL.
- Simulation of the transient locking response.

The applet is similar to a spreadsheet. Data is entered in the editable cells. The input data consist of frequencies, division ratios, noise parameters, targeted cut-off frequency for the PLL or the description of the loop filter. The results of calculations are displayed in the non-editable cells, and in different graphs that show the AC response of the PLL, the SSB output phase noise and the transient locking response. The results are automatically updated when pressing the Enter key. Help on context can be obtained by clicking the headers of the cell group.

4.5.2 Background on PLL’s

The PLL is a feedback circuit that locks the phase and the frequency of a Voltage Controlled Oscillator (VCO) to a reference oscillator, usually of high spectral purity. A PLL can have various applications but we consider here more particularly the application of PLL’s to frequency synthesis, i.e. generation of a signal with a frequency that is a programmable multiple of the reference oscillator frequency.

The reference oscillator is the starting point of the PLL. Its frequency is usually divided to a lower frequency called comparison frequency, because this is the frequency at which the phase comparison is performed. The frequency divided reference signal is one input of the phase comparator. The other is obtained from a frequency division of the RF oscillator signal. When the PLL is locked, the two inputs of the phase comparator are at the same frequency. It results immediately that:

- fRef / m = fRF / n = fcomp

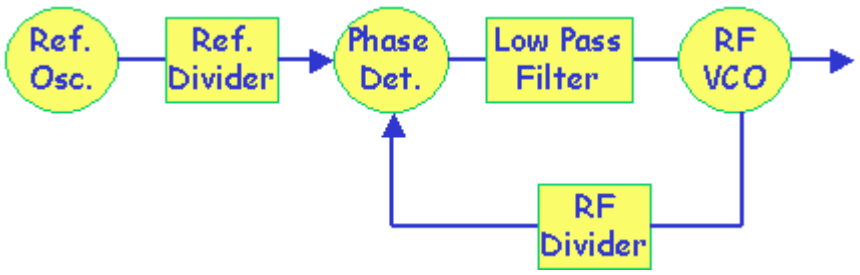


Fig 9. Basic PLL block diagram

where m is the frequency division ratio of the reference oscillator, and n is that of the RF VCO. If n is an integer number, the RF frequency can only be an integer multiple of the comparison frequency. Therefore in that case, the comparison frequency is determined by the frequency step that is desired at RF. In a fractional N PLL, the RF frequency can be a non integer multiple of the reference frequency. This is generally achieved by modulating the division ratio between two adjacent integer values.

The phase detector is the key element of the PLL. Several types of phase detector are possible but we consider in this PLL model a phase-frequency detector with a charge pump as output circuit. This kind of detector is the most common in modern PLL. It is frequency sensitive, i.e. able to deliver an average current of the same polarity as the frequency error. This property ensures convergence towards the wanted frequency even if the initial frequency error is large. The charge pump output circuit of the detector delivers current pulses of constant amplitude but with duration proportional to the phase error.

4.5.3 Input variables, Frequencies and division ratios

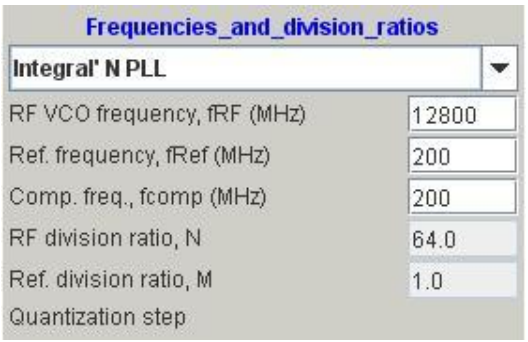


Fig 10. VCO and Reference Frequency input field

The type of PLL you want to design and simulate, for TFF1003HN this is an integral N, is the first choice that is requested in this spreadsheet. Then, you must specify the operating frequencies of the PLL:

The frequency of the RF VCO, fRF;

- The frequency of the reference oscillator, fRef ;
- The comparison frequency, fcomp.

The appropriate division ratios to get from fRF or fRef down to fcomp are automatically calculated.

The PFD for the TFF1003HN is running at the reference frequency hence the Ref. freq. and the Comp. Freq. must have the same value.

4.5.4 The PLL Loop Filter

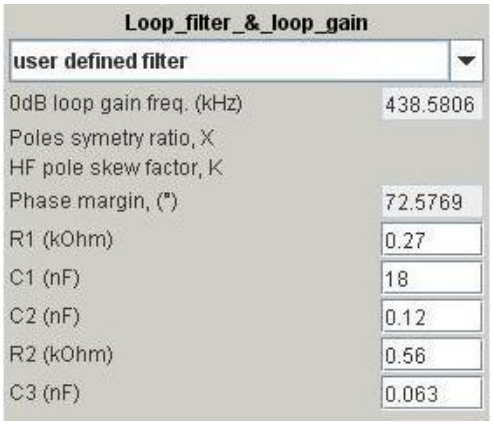


Fig 11. Loop-filter input field

By selecting filter design (3rd or 4th order) the package will calculate / propose a filter with sufficient phase margin. See figure 7 from section 3.4 for loop-filter configuration. Switching over to user-defined filter enables a user to play with the actual component values. Please keep in mind that the minimum value for C3 is 30pF (no external capacitor placed) as this value is integrated inside TFF1003.

The loop filter determines the frequency bandwidth of the PLL. You can select either a 2nd order or 3rd order passive filter. The relevant transfer function is the trans-impedance of the filter, the input signal being the output current from the charge pump, the output being the voltage applied to the VCO. The figure below shows a third order filter.

The loop circuit, consisting of the phase detector, charge pump, filter, VCO and RF divider, has an open loop frequency response as indicated in the figure on the right. In design mode, the RC components of the filter are automatically determined from the unity gain frequency f0, i.e. the frequency at which the loop gain is 1 in linear, or 0 dB. The unity gain frequency of the PLL will be about of the same order of magnitude, but its exact value will depend on the parameter X called 'symmetry ratio' . This parameter controls the position of the zero fz and of the high frequency pole(s) fp of the loop transfer function with respect to f0. The location of pole(s) and zero is determined by:

$f0 / fz = X$

$fp / f0 = f(X)$, with $f(X) = X$ for a second order filter.

Moving fz and fp closer to f0 decreases the phase margin. The PLL response exhibits a higher overshoot and can become unstable. Moving fz and fp apart from f0 improves the phase margin. The overshoot is reduced or disappears, the stability gets better. The optimum value of X is about 2.7 to 3 for achieving a good stability and the minimum locking time.

For a second order filter, there is only one high frequency pole at frequency fp. If a third order filter is selected, there are two high frequency poles. Their location with respect to the optimum pole frequency fp is determined by the parameter k according to :

fp1 = (1-k)*fp

fp2 = (1+k)*fp

In simulation mode, you specify the components of the filter. The applet calculates the unity gain frequency of the loop and the corresponding phase margin.

4.5.5 Gains

The open loop gain of the PLL is the product of the gains blocks in the loop. Therefore the gains of the phase detector and of the RF VCO must be specified to enable calculation of the appropriate loop filter.

The phase detector gain **Kd** is calculated from the sink/source current amplitude **Ipeak**. The gain relates the average current delivered over one period of the comparison frequency, to the phase difference of the input signals of the phase detector. For a conventional phase-frequency detector as assumed in the PLL model, the detector gain, in mA/radian, is given by:

- Kd = Ipeak / (2*pi)

This expression comes from the fact that a phase difference of 2*pi, which means a time difference of one period of comparison, results in a current pulse of length also equal to one period of the comparison frequency. For an error of 2*pi, the average output current over one comparison period is therefore Ipeak. For a smaller phase error, the pulse length is reduced proportionally.

The RF VCO gain **Kvco** specifies how fast the VCO frequency varies with the control voltage. A linear tuning characteristic is assumed for simplification. The VCO gain has the dimension of MHz/V.

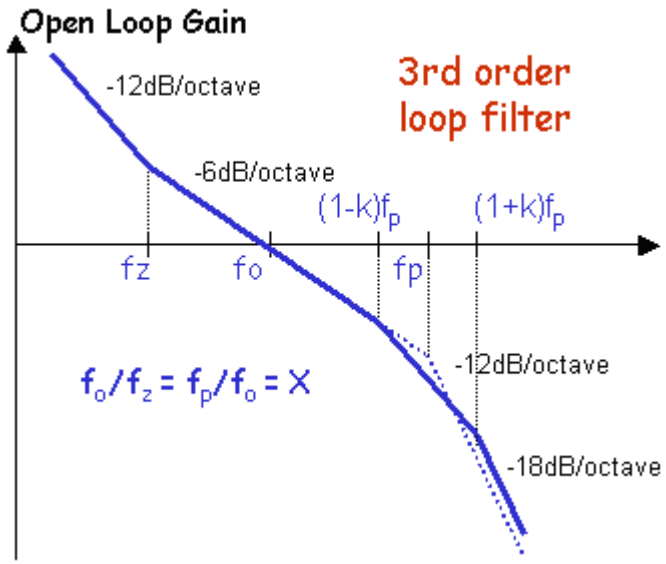


Fig 12. Figure title here

4.5.6 RF VCO noise

The RF VCO phase noise is assumed to decrease by 30dB/decade close to the carrier, then by 20dB/decade until the noise floor is reached. The characteristic is specified by giving the corner frequencies and the corresponding phase noise. The 30dB corner frequency is the offset frequency at which the slope changes from 30 to 20dB/decade. The 20dB corner frequency is the offset frequency at which the noise floor is reached.

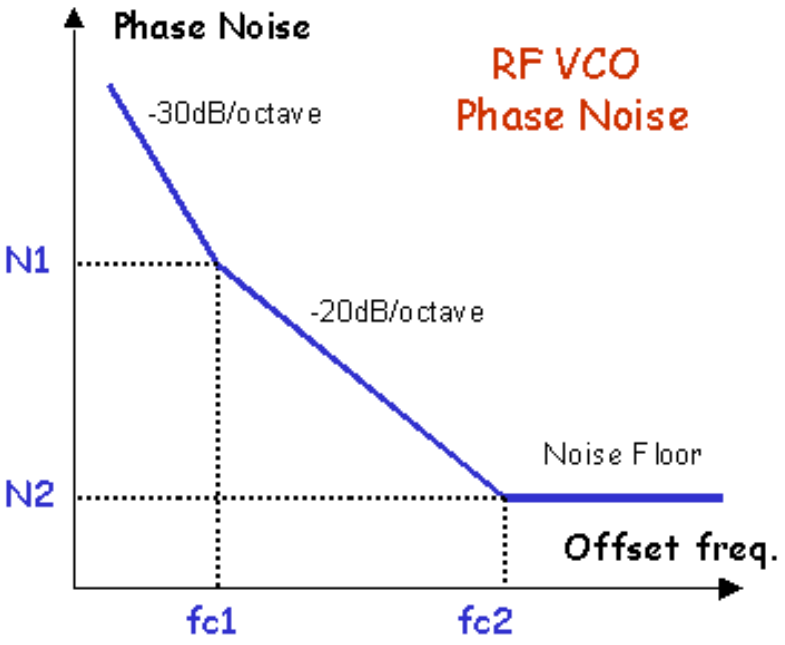


Fig 13. Figure title here

4.5.7 Reference noise

The phase noise of the reference path is assumed to decrease by 20dB/decade very close to the carrier, until the floor is reached. The characteristic is described by the corner frequency at which the noise floor is reached, and the corresponding phase noise. This model is used to represent not only the noise of the reference oscillator but includes also the contribution of the reference amplifier.

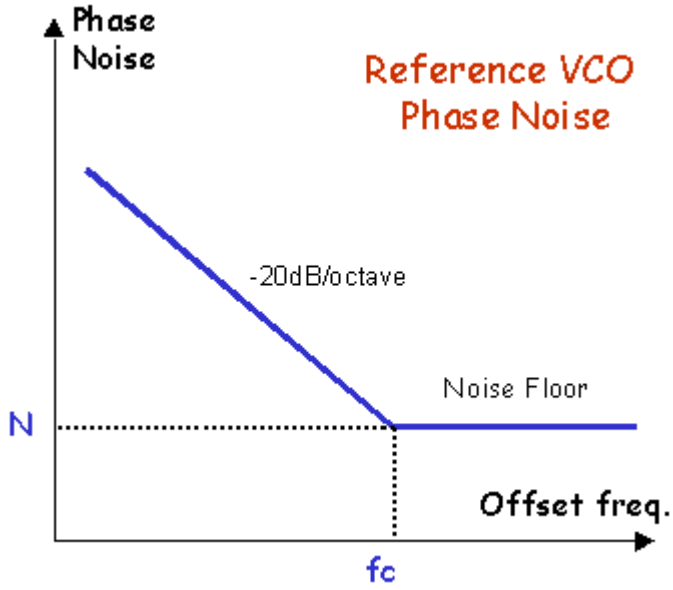


Fig 14. Figure title here

4.5.8 Divider and PFD noise

The phase noise of the dividers is referred to the comparison frequency.

The noise of the phase detector (PFD) is also referred to the comparison frequency. It does not include the noise of the charge pump which is treated separately. This is the noise of the flip-flop circuits implementing the phase-frequency detection function.

4.5.9 Charge pump parameters

The noise current of the charge pump is an input parameter of the PLL noise model. It can be extracted from a Pnoise simulation in locked state conditions (zero average current over a period of comparison).

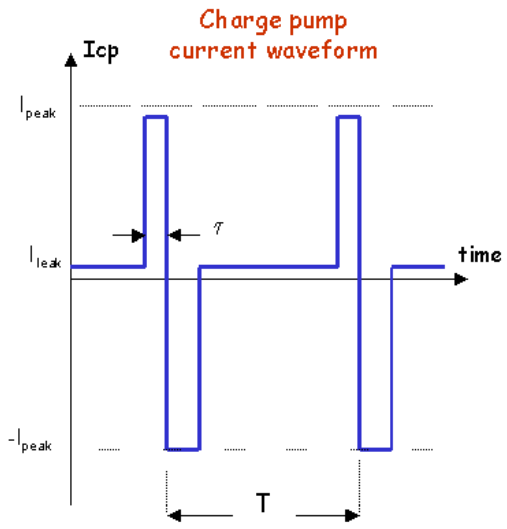


Fig 15. Figure title here

For calculation of the comparison frequency breakthrough (tone at distance equal to comparison frequency in the PLL output spectrum), a charge pump current waveform as indicated in the picture on the right is assumed. It accounts for practical limitations which make the occurrence of very narrow up/down current pulses unavoidable. In the model, the zero average current waveform characterizing the locked state is modeled as two adjacent up/down pulses of equal areas, with duration **Tau** and height **Ipeak**. In case of DC leakage, the current pulse with opposite sign to the leakage current is extended in order to maintain a zero mean current. The comparison frequency breakthrough at PLL output is calculated by applying the loop filter and VCO transfer functions to the spectral component at comparison frequency contained in the charge-pump waveform.

The breakthrough is calculated in integral N mode only. For a fractional PLL, tones in the output spectrum are more difficult to calculate analytically. Their level and position depends on the fractional division ratio and on the statistics on the divider modulation signal. Therefore no calculation of output tones is done for a fractional PLL in this tool.

4.5.10 Graphs

There are 3 graphs which can be displayed, but one at a time, using the choice bar. The graphs are the following:

- **PLL gain** : this graph displays the phase response of the PLL at the output of the RF VCO, using a linearized model of the PLL.
- **PLL noise** and its contributions : using the noise parameters of the PLL building blocks entered by the user, the SSB phase noise at the VCO output is computed using the above mentioned linear model of the PLL.
- **PLL locking** (response to a frequency jump) : the model assumes a **pulse width modulated error signal**. This is more accurate than continuous time and sampled linear models generally assumed, yet not fully exact since the error pulse is modulated both in width and position in a real PLL. The difference is depicted by the figure on right. In the model, the pulse always starts at the beginning of a comparison period, whereas it can start earlier in an actual PLL when the feedback signal is in advance.

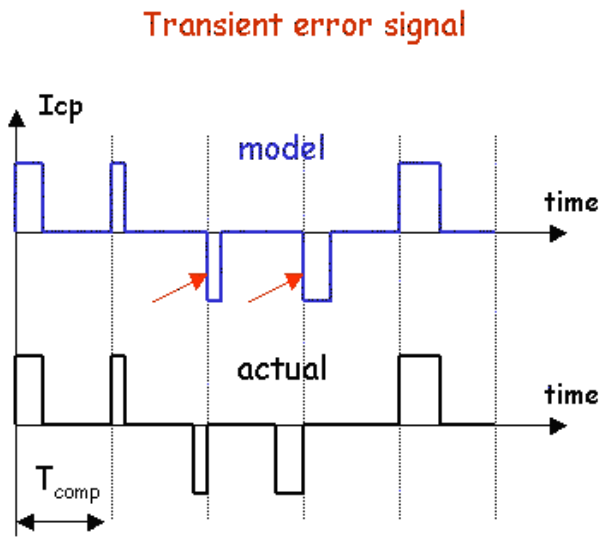


Fig 16. Figure title here

4.5.11 Input values for the TFF11xxxHN PLL properties (example for 12.8GHz):

Detector_and_RF_VCO_gains	
Sink/source current, Ipeak (mA)	1.0
RF VCO gain, Kvco (MHz/V)	670
Detector gain, Kd (mA/rad)	0.1592
RF_VCO_noise_parameters	
30dB slope corner freq.(MHz)	0.01
Corresponding noise (dBc/Hz)	-70
20dB slope corner freq.(MHz)	25.0
Corresp. noise floor (dBc/Hz)	-137.9588
Reference_noise_parameters	
20 dB slope corner freq.(MHz)	0.001
Corresponding noise (dBc/Hz)	-150
Dividers_and_detector_noise	
RF div.noise at fcomp, (dBc/Hz)	-200
Ref.div.noise at fcomp, (dBc/Hz)	-200
PFD noise at fcomp, (dBc/Hz)	-200
Charge pump parameters	
Ch.pump noise current, (pA/vHz)	32
Minimum pulse length, Tau (nS)	1.0
Leakage current, Ileak (nA)	0.1
Spur at comp. frequency (dBc)	-78.1748

Fig 17. Detector and RF VCO gains input field

Those values are derived from system simulations and measurements.

It is assumed that the charge pump noise current is one of the dominant noise sources, this value [pA/SQRT(Hz)] should be adapted in case another divider ratio is used

Noise from the frequency divider is hardly contributing to the total noise hence its value is set to –200dBc/Hz.

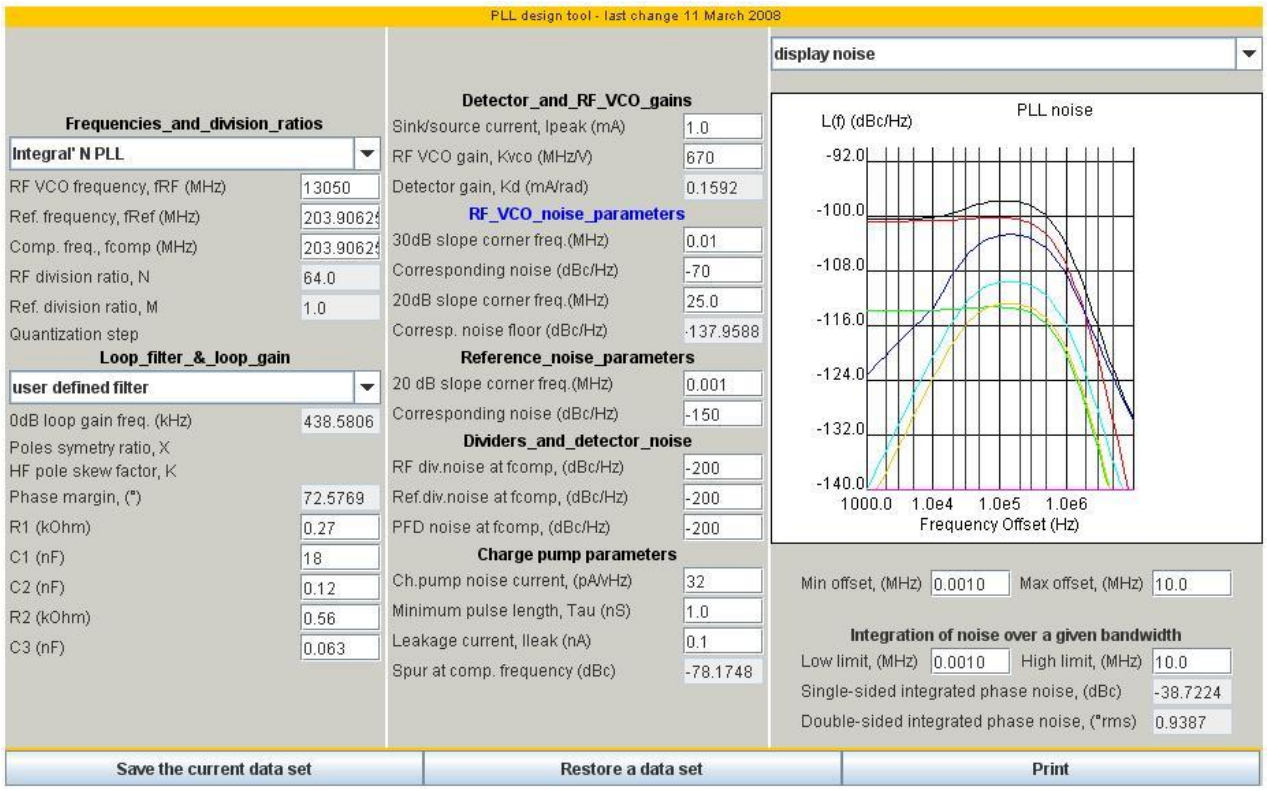


Fig 18. Overall PLL design cockpit, example at 13.050GHz

4.5.12 Loop-filter BW and Phase Noise / Phase Jitter /Ref. spur relations

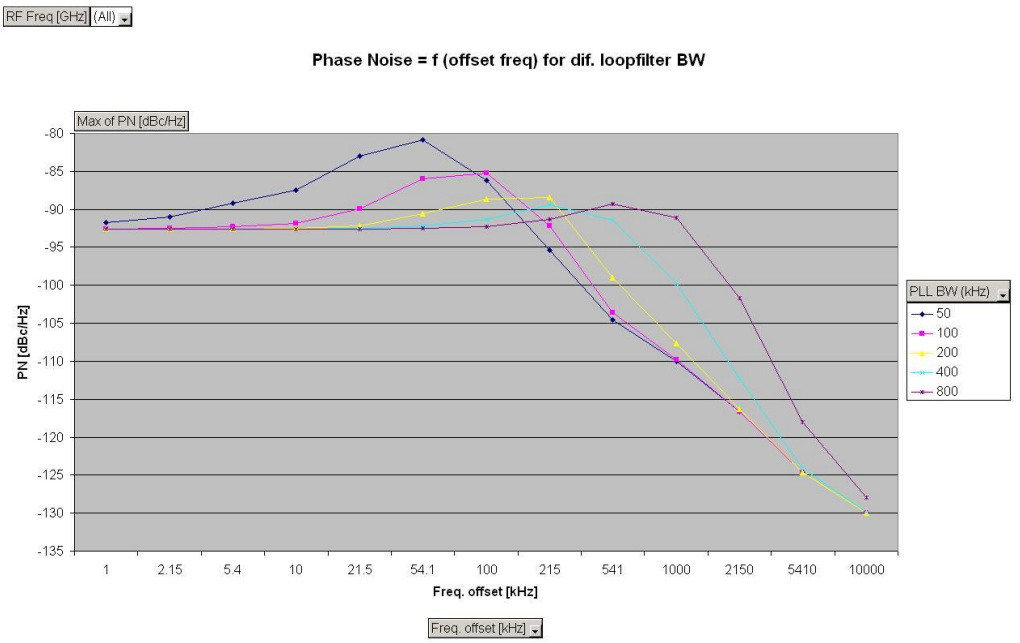
In the next three graphs we can see the influence of the loop filter BW on:

A) the PN = f (freq) behavior [figure 19]

B) the PJ = f (loop filter BW) [figure 20]

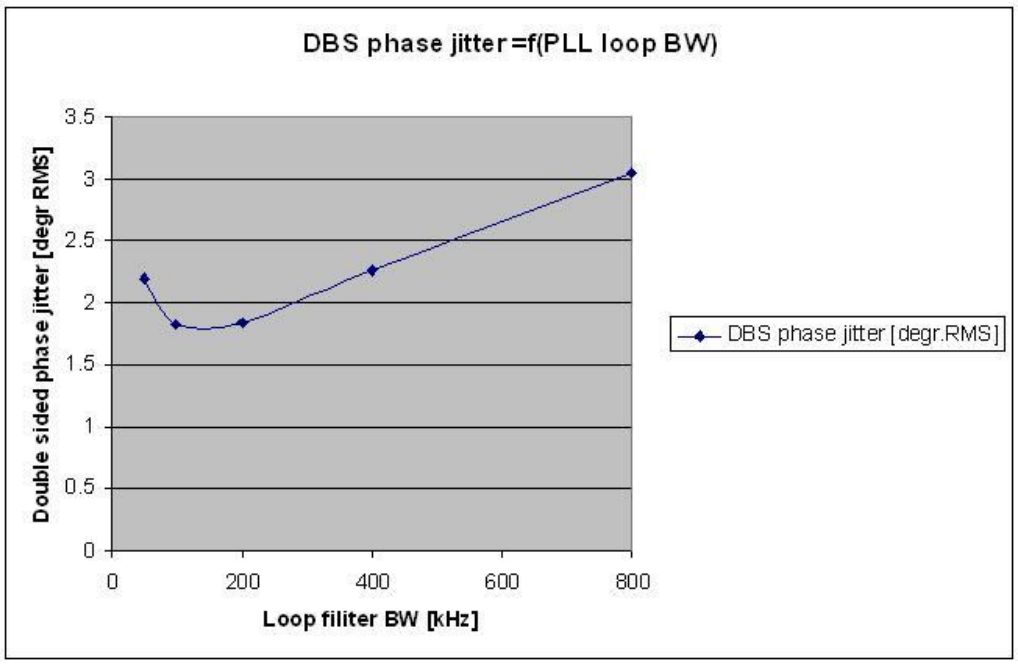
C) The Ref. spurious = f (loop filter BW) [figure 21]

Depending on the system requirements the optimum can be chosen.



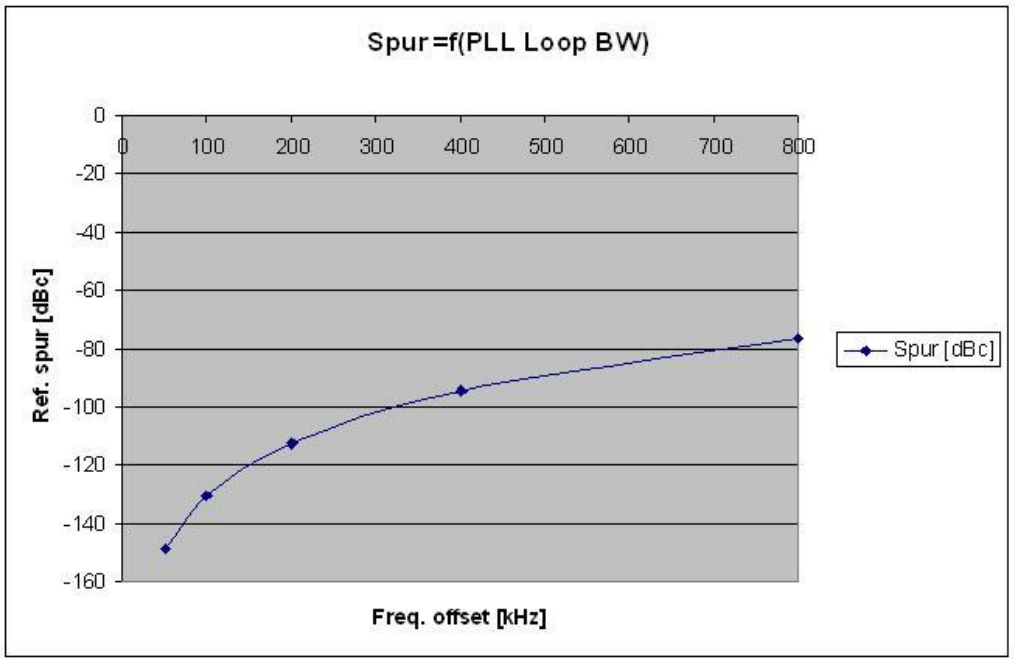
(1)

Fig 19. 12.8GHz Loop Filter BW influence on phase noise, N=64



(1)

Fig 20. 12.8GHz Loop Filter BW influence on RMS phase jitter, N=64



(1)

Fig 21. 12.8GHz Loop Filter BW influence on ref. spurs, N=64.
Remark: actual performance not only determined by loop filter design.

5. Typical EVB Results

Table 2 typical results measured on the Evaluation Boards.
Operating Frequency 13.050GHz; Vcc = 3.3V; Temp = 25 °C, unless other wise specified.

Parameter	Symbol	TFF11XXX EVB	Unit	Comment
RF output level	Pout	-4.8	dBm	
Phase noise	PN	-99	dBc/Hz	At 100kHz offset
Phase jitter	PJ	0.71	°RMS	Integration interval from 1kHz till 1MHz
Tuning Voltage	Vtune	1.657	Volts	Measured at output freq. 13.05GHz (div ratio 16,32,64)
Tuning Voltage	Vtune	1.994	Volts	Measured at output freq. 12.80 GHz (div ratio 128,256)
Tuning Slope	slope	-673	MHz/V	Higher freq. is lower tuning voltage!
Supply current	Icc	96	mA	Total current for EVB

5.1 Phase noise plots

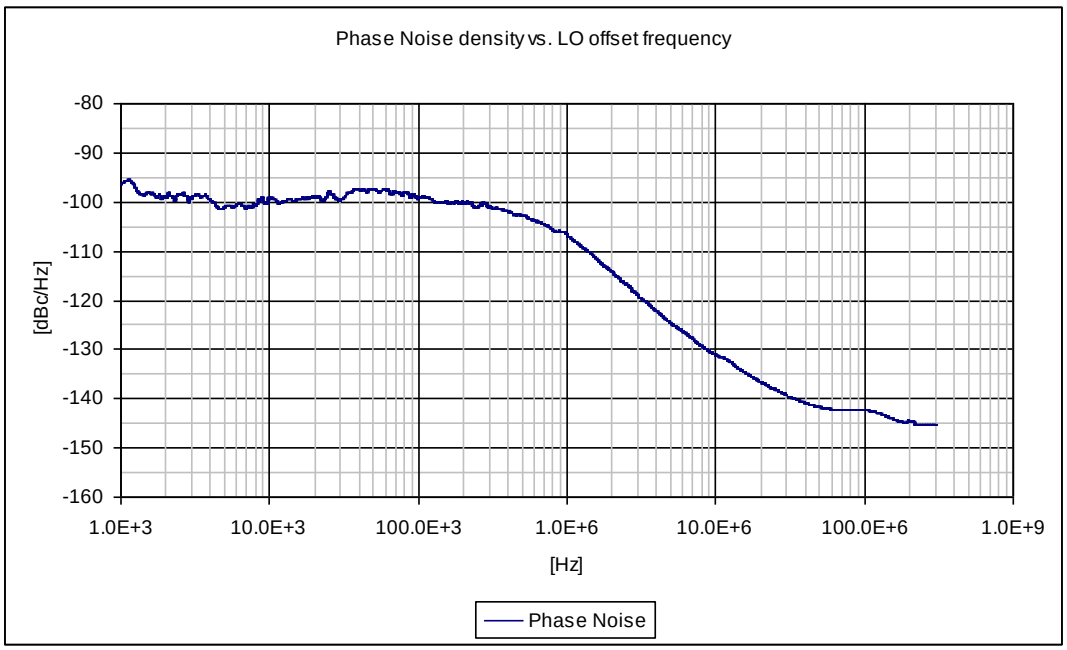


Figure 5.1 Phase noise at 13.05GHz, N=64

Table 3: typical settings used for figure 6 “PN graph”

Test:	**PhaseNoise Measurement**	
P reference:	0	dBm
LO Frequency:	13050	MHz
Power Vcc:	3.3	V
Power Icc:	94.9	mA
PhaseNoise:	0.71	deg
VCO phase noise @ 10MHz	-131.16	dBc/Hz

5.2 Spurious emissions, small band

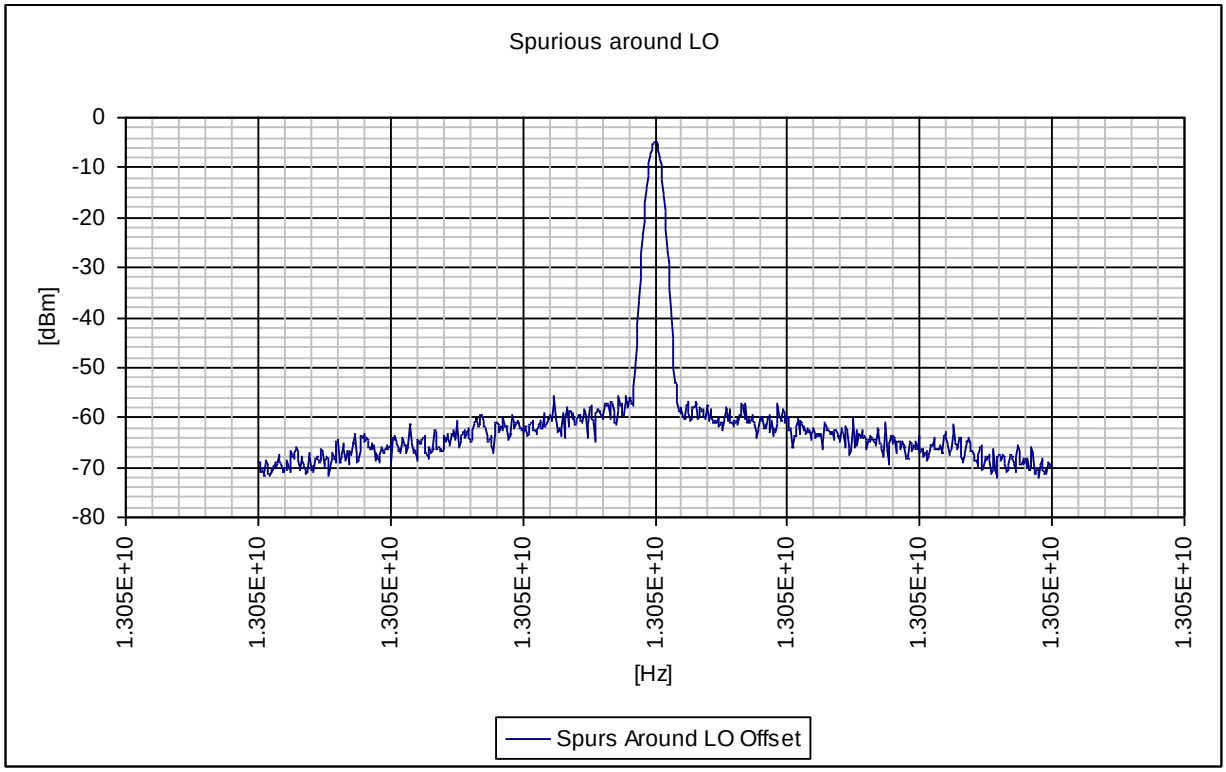


Figure 5.2 Small band spurious at 13.05GHz, N=64

5.3 Reference spurs

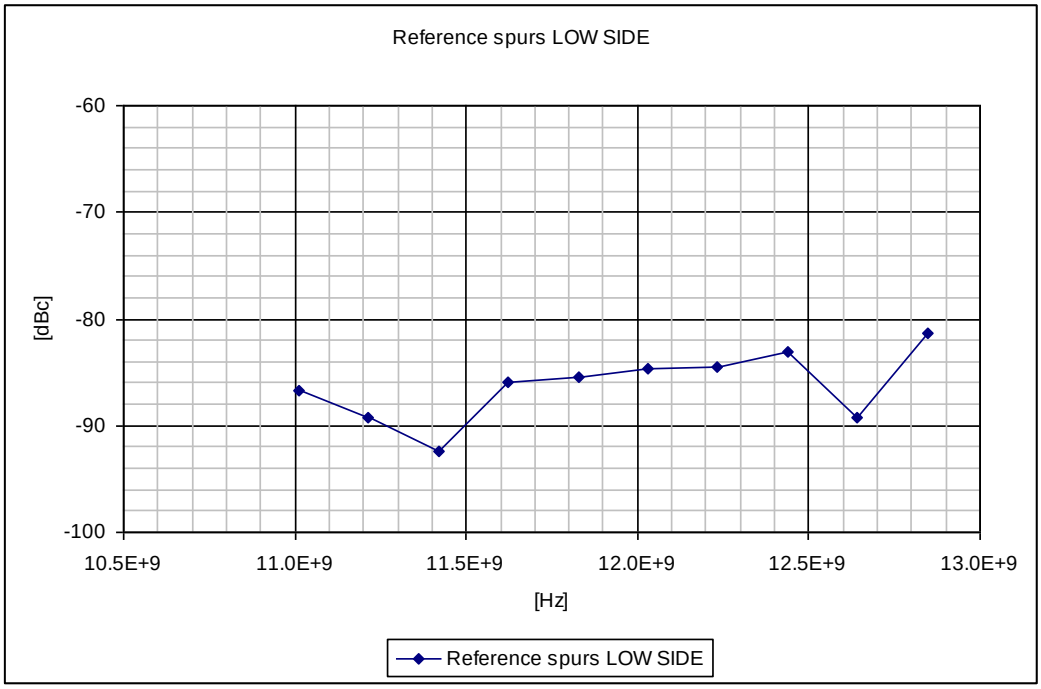


Figure 5.3.1 Ref. spurs Low Side at 12.8GHz, N=64

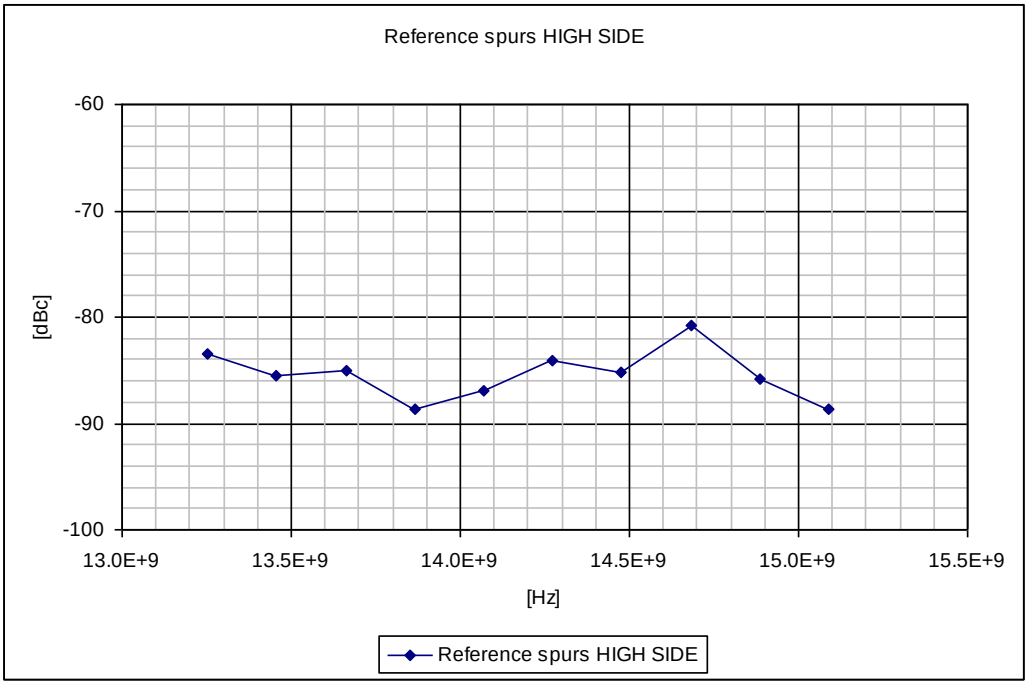


Figure 5.3.2 Ref. spurs High Side at 12.8GHz, N=64

5.4 IF spurs

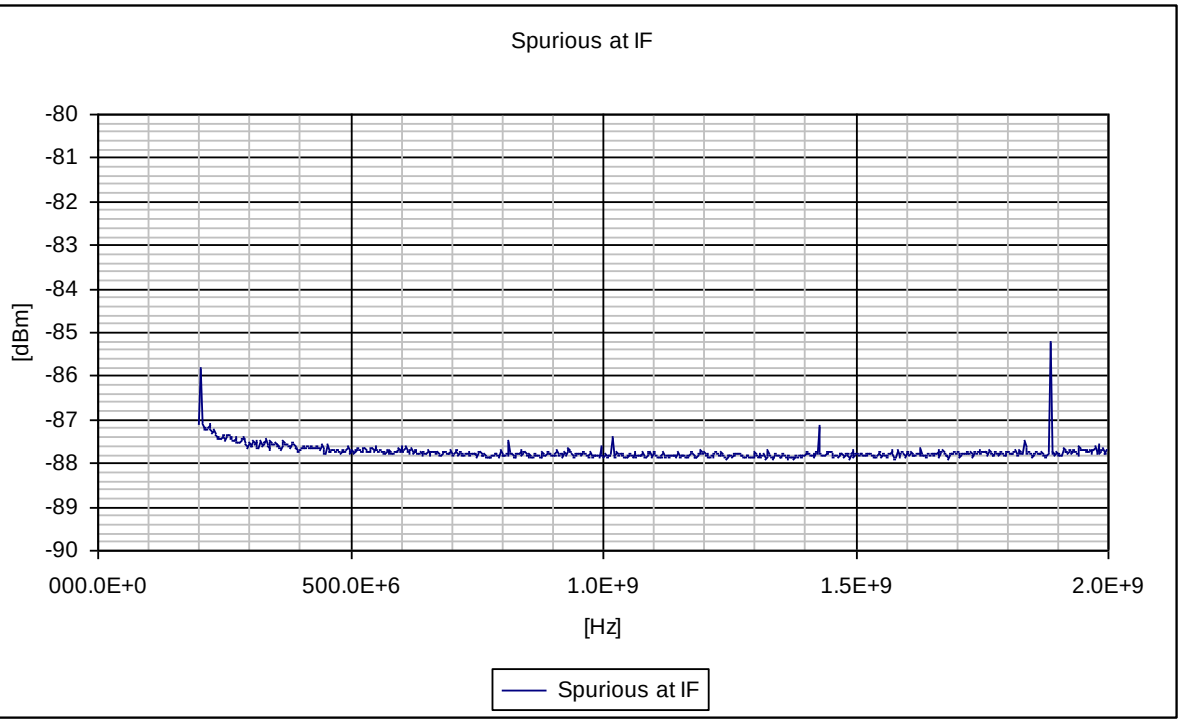


Figure 5.3.1 IF spurs at 12.8GHz, N=64

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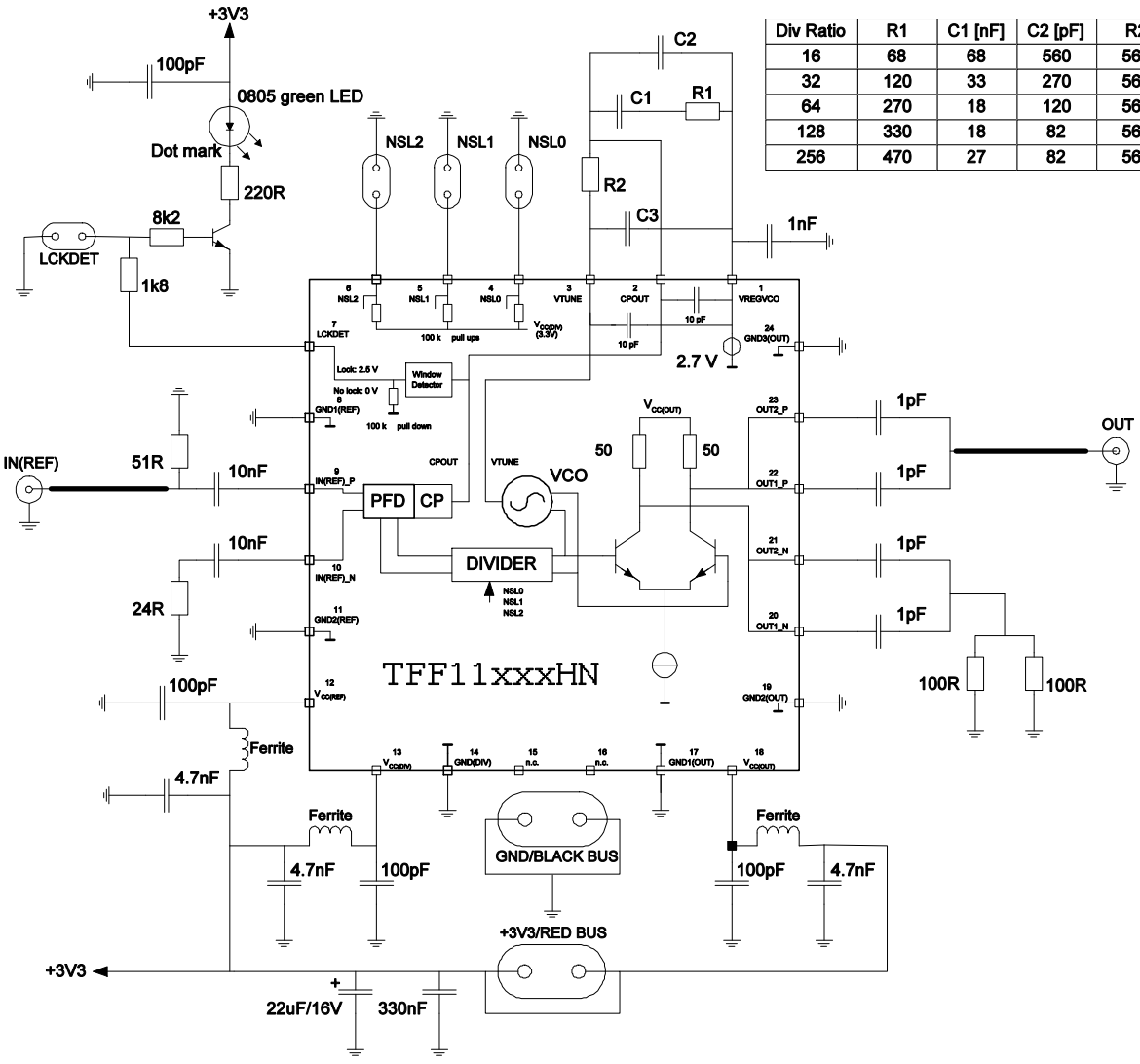
continued >>

9. Appendix 1: EVB schematics



Div Ratio	R1	C1 [nF]	C2 [pF]	R2	C3 [pF]
16	68	68	560	560	33
32	120	33	270	560	33
64	270	18	120	560	33
128	330	18	82	560	33
256	470	27	82	560	33

Fig 22. Figure title here

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Appendix 2: EVB BOM

Component type	Supplier	Part number	Value	Comp. count
Resistor 0402	various		100R	2x
Resistor 0402	various		51R	1x
Resistor 0402	various		24R	1x
Resistor 0402	various		1k8	1x
Resistor 0402	various		8k2	1x
Resistor 0603	various		220R	1x
Resistor 0402	various		150R (for N=64)	1x
Resistor 0402	various		510R	1x
Capacitor 0402	various		1pF NP0	4x
Capacitor 0402	various		10nF X7R	3x
Capacitor 0402	various		100pF NP0	4x
Capacitor 0402	various		4.7nF X7R	3x
Capacitor 0805	various		330nF X7R	1x
Capacitor 0402	various		39nF X7R (N=64)	1x
Capacitor 0402	various		300pF (N=64)	1x
Capacitor 0402	various		47pF	1x
Electrolytic Cap	various		22uF/16V	1x
Transistor	NXP		BC848B	1x
SMD LED 0805	Various		Don’t care	1x
Double header pitch 2.54mm	Various		Don’t care	4x
Banana socket			One black, one red	2x
LO generator IC	NXP		TFF11xxxHN	1x
SMA connector				2x

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