UM TFF100x / TFF11xxx clean-up PLL

Example design to generate CW ref. signal for TFF1xxxx and lock to external clock

Rev. 2.0 updated Rev. — 20/10/2010 **User manual**

Document information

Info	Content
Keywords	Clean-up PLL, Synthesizer, micro-wave Local Oscillator, VCXO, PLD, TFF1003HN, TFF11xxx
Abstract	Document that describes the design- and implementation phase and the usage of the Clean-up PLL demonstrator. This demonstrator can generate a reference signal (CW) for the NXP TFF100x/TFF11xxx series of LO generators. It also includes “frequency tracking” functionality to enable tracking to an external 10MHz reference.

Revision history

Rev	Date	Description
0.1	20100217	First draft revision
0.2	2010 Sep 15	Second draft updated
1.0	2010 Oct 20	First version after review M.G. and T.B.
1.1	2011 May 16	Corrections on calculating PN and required ref. PN added (section 3.2.4)
2.0	2012 Oct 3	Improvements at BPF/VCXO=>PLD based on experiences at low temperature added, contact at TST changed

Contact information

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1. Introduction

The TFF1xxxx clean-up PLL demo board (CUP) is a platform designed to generate the required reference signal (CW) for one of NXP LO generators from the TFF1xxxx range. Applicable products are:

- TFF1003HN (for VSAT applications, 12.800 – 13.050 GHz)
- TFF1007HN (VSAT applications, 14.75GHz)
- TFF1008HN (VSAT applications, 14.275GHz)
- TFF11xxx (frequency ranges from 7.0GHz till 15.2GHz)

For more details please refer to the appropriate datasheet and/or user manual for corresponding product demo-board. Available user manuals are:

- UM TFF1003HN
- UM TFF1007HN, draft
- UM TFF11xxx, draft

Above mentioned LO generators include an “integer N PLL” with fixed divider ratio (HW programmable to 16, 32, 64, 128 or 256) hence require a reference signal in the range from 27MHz to 950MHz depending on the applicable requirements.

Please note that the TFF100x/TFF11xxx reference signal properties depict directly the LO signal quality with respect to frequency stability and spectral purity (phase noise).

Besides generating the required reference signal this demo-board also has the functionality to keep the reference frequency in “frequency-lock” with an external reference clock as required for many VSAT block UP converters (BUC).

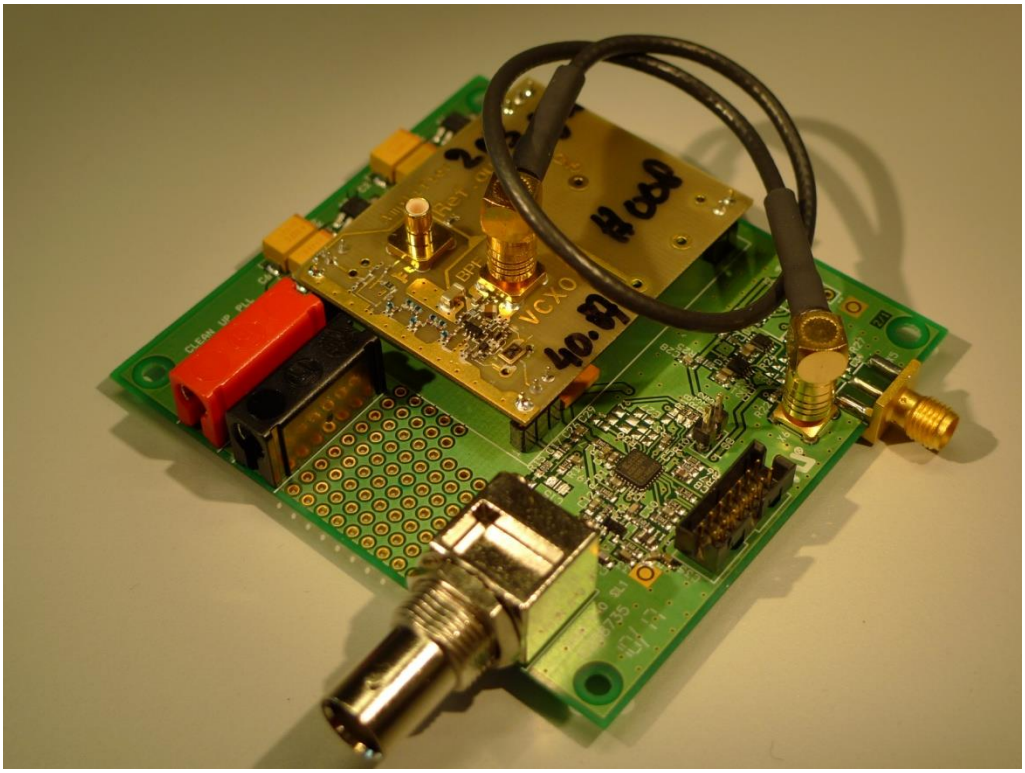

Fig 1. Clean-up PLL demonstrator with 203.90625MHz VCXO module

1.1 Definitions / Assumptions

The TFF100x/11xxx series LO generators are intended to generate a fixed LO in the μ-wave frequency range. Making it programmable (within given frequency range) in one application is outside the scope of this document.

For most of the examples in this document the VSAT application with 13.05GHz LO locked to an external 10MHz clock is used, however the whole LO frequency range, and corresponding reference frequency range, is feasible by this concept.

As this demonstrator is initially designed for VSAT applications the frequency tracking range is limited, when more tracking range is required a suitable VCO should be designed as this block is dominating the frequency tracking range currently.

1.2 Functional requirements for clean-up PLL

The clean-up PLL should generate required reference frequency with suitable level to drive the TFF1xxxx demo-boards. This reference frequency should lock to an external connected reference clock, target frequency 5MHz or 10MHz, level 0dBm typical, sine wave (CW), source impedance 75Ohms.

The spectral purity of the reference frequency should be significantly below the TFF1xxxx synthesizer noise floor, for VSAT μ-wave application this is <-140dBc/Hz at 100kHz offset.

The clean-up PLL should be capable of delivering any output frequency in the 27MHz to 950MHz frequency range.

2. CUP Design Considerations

2.1 Functional description

Main functionality for the demonstrator is to generate the reference for applied LO generator, which worse case could be a sine wave or preferred a clipped sine wave (for optimum phase noise properties steep edges are preferred).

This reference signal has to be frequency locked to applied reference clock (10MHz or 5MHz) by comparing the frequencies and generating an error signal. Since the required reference frequency is not necessarily a multiple of the reference clock a kind of “fractional N” PLL has to be implemented. Preferred architecture is such that the required divider ratios can be easily modified (in software), and that the entire (possible) frequency range can be covered in one concept.

2.2 Target specifications

First version of the demonstrator should be targeted for VSAT, TFF1003HN N=64 13.050GHz LO frequency, application. Later other reference frequencies should become available (derived from the same concept). Required phase noise for VSAT BUC is –95dBc/Hz at 100kHz offset.

Reference output

Output frequency: see table 1 for possible configurations, 203.90625MHz for VSAT BUC

Reference output phase noise: see section 3.2.3, for VSAT BUC typical –148dBc/Hz at 100kHz offset

Lock range: +/- 25ppm over entire temperature & supply range

We can differentiate two sets of requirements for Pout/Vout/Zout, one for the demonstrator and one for an application that contains all functionality on one PCB:

2.2.1 Requirements for demonstrator platform

Output power: –10dBm < Pout < 0dBm

Output impedance: 50 Ohms to enable evaluations by coaxial cables

2.2.2 Requirements for one PCB LO generation platform

Output voltage: 100mVpp < Vout < 600mVpp

Output impedance: low, should be optimized to obtain maximum Vout to TFF1003 reference input (which is high Z).

Reference clock input

Input frequency: 5MHz or 10MHz (other frequencies possible by changing VHDL code)

Input level: 0dBm

Input impedance: 75 Ohms

Reference clock PN: <=-135dBc/Hz at 1kHz offset, <=-140dBc/Hz at 10kHz offset

DC supply requirements

Supply voltage: 5 Volts (on board 3.3V and 1.8V are generated to feed logic and VCXO)

Supply current: <150mA

2.3 Architecture choice

In figure 2 we can see the basic block diagram for an integer N solution.

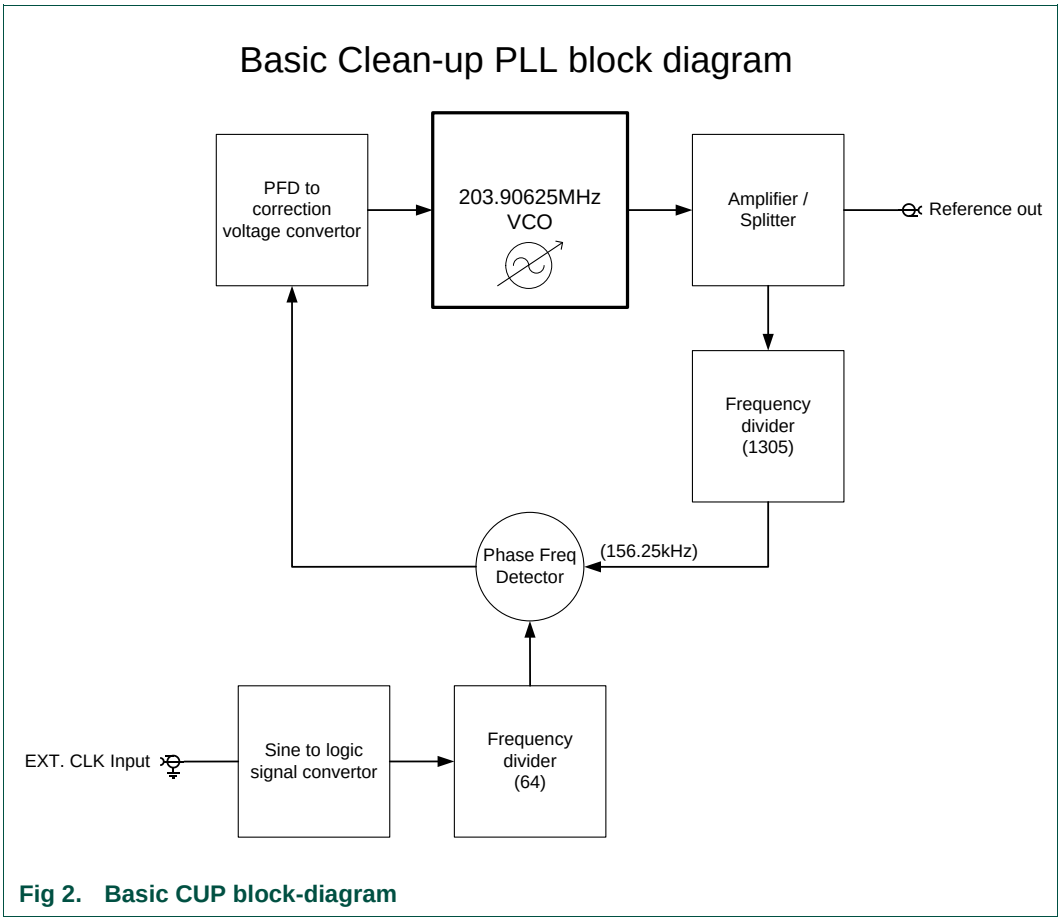

Fig 2. Basic CUP block-diagram

Input for the CUP is the external system clock. This, 10MHz or 5MHz, CW signal is converted to a logical signal and then divided and fed to the PFD. The main block is the VCO from which the output frequency is also divided down to the same frequency as the divided 10MHz reference. Then both are compared in the PFD and the PFD output is fed into a block that converts it to a usable error-signal/control signal for the VCO.

For practical implementations the choices for the “logic” blocks are:

a) Implement every block in logic circuits;

b) Implement dividers and PFD in a (fractional N) PLL IC;

c) Implement dividers and PFD in a programmable logic device (PLD).

Option a) could be preferred for cost optimization but will be PCB space consuming and not flexible. Option b) is a good alternative although it requires a logic device (i.e. PIC processor) to program the PLL divider ratio(s) every time the application is switched on.

We have chosen for option c) as a good compromise between board space, flexibility, BOM and power dissipation.

2.4 Basic required building blocks

What are the required building blocks for the CUP? Each block will be briefly described in the following sections.

2.4.1 VCO (or VCXO)

Because the VCXO/VCO functionality for the entire 7 – 15GHz frequency range, as dictated by the TFF11xxx reference signal range, could not be met with one design it was decided to implement a VCO/VCXO subassembly. This enables the user to test different kind of VCO's on this platform. Output of this block is a CW signal, for example a clipped sine-wave (CW), with sufficient phase noise (PN) to meet required LO PN. Input is a control voltage that set's, within the required range, the fundamental frequency of the VCO.

2.4.2 Amplifier converter for the external clock

The external clock could be a CW signal ranging for example from –10dBm till +5dBm (50Ohms). This needs to be amplified/converted to a signal that can be taken as input for the frequency divider.

2.4.3 Amplifier / splitter /converter for the reference signal

Depending on the output level and load capabilities of the VC(X)O additional amplification might be required. Also the signal should be divided into two paths, one towards the external reference input of applied TFF11xxx, the other towards the frequency divider.

2.4.4 Frequency dividers

The VC(X)O frequency as well as the reference clock should be divided into a lower frequency signal in order to be processed by the PFD. This can be a basic digital (binary) counter. To accommodate the whole frequency range (7-15GHz) the maximum divider ratio should be sufficiently large.

2.4.5 Phase Frequency detector

Required to obtain frequency lock between the reference and external clock frequency. For most applications a frequency detector will also do the job.

2.4.6 PFD to correction voltage converter (loop-filter)

Depending on the PFD implementation the output signal (usually pulses) needs to be converted to a control signal that can be used by the VC(X)O. Also the loop-stability should be obtained by this circuitry.

3. The NXP CUP demonstrator implementation

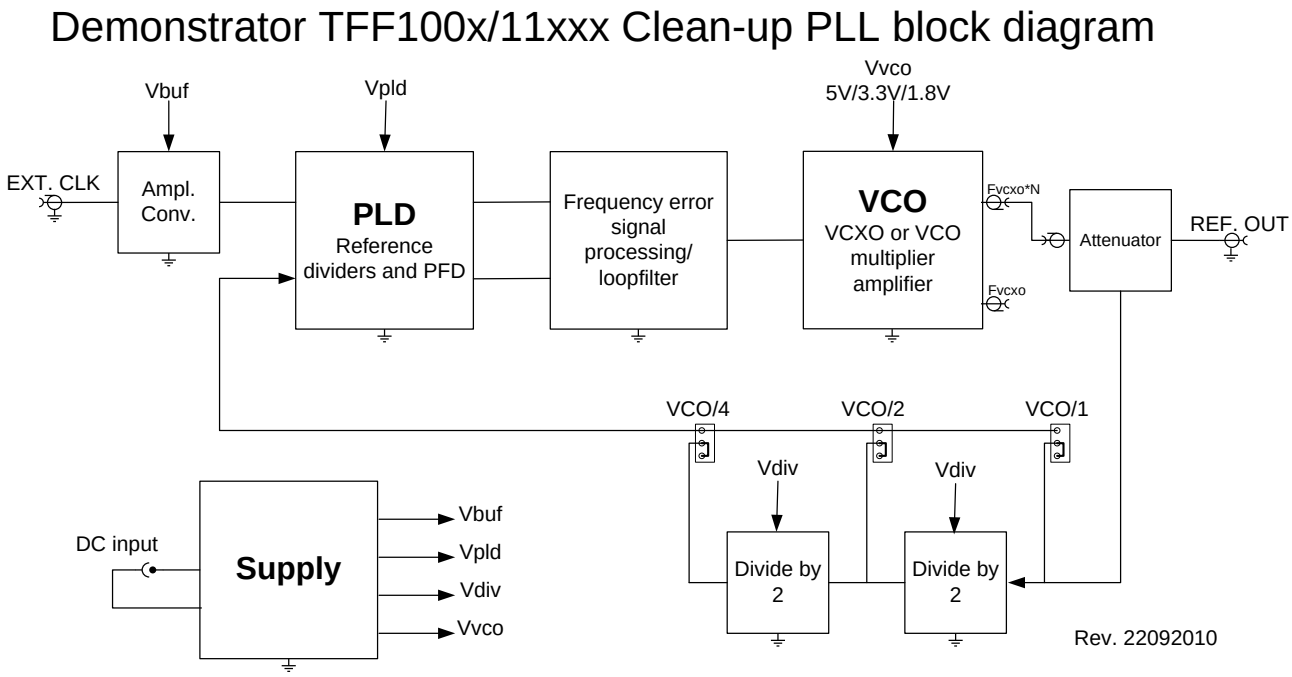

Fig 3. NXP demonstrator's block-diagram

3.1 NXP's CUP demonstrator implementation

In the NXP demonstrator implementation the VCXO works at a fraction of required reference. The VCXO frequency is multiplied before it is fed into the LO generator reference input. The VCXO signal and the reference clock are fed into a programmable logic device (PLD). This allows various implementations of frequency dividers and PFD by programming the PLD.

Choosing a PLD also has the benefits that it can run autonomously (no need for programming the required divider ratios every time after start-up) and can be relatively cheap.

Before the reference clock enters the PLD it is amplified and converted to a DC coupled signal. This is required as the "zero crossings" in the reference clock should be detectable to generate the logic ref-clock signal.

Used configuration inside the PLD is such that the VCXO clock and the reference clock are divided until a common frequency is reached. The divided VCXO and clock signals are then fed into a phase-frequency-detector (PFD). The outputs of the PFD are transformed to a charge pump which gives positive or negative current pulses. Those pulses are filtered (integrated) by an external PLL loop-filter in order to suppress the comparison frequency energy (also known as reference breakthrough) and to stabilize the PLL process.

Example:
assuming a reference carrier (for the TFF1003HN LO generator) at 203.90625MHz and

divide it by 1305, this will give a block signal at 156.25kHz. When we divide the reference clock (10MHz) by 64 we also get 156.25kHz, both divided signals can be compared in phase/frequency to generate the error signal.

To cover all NXP LO generator reference frequency requirements in one concept, see table in section 8.1) the VCO frequency requirements dictate a very high tuning range (27MHz to 950MHz) which is practically unfeasible in one concept. For this reason a modular approach was chosen.

We recommend using a VCXO for reference frequencies up till approximately 60MHz (the frequency at which fundamental crystals can be bought). Crystal oscillators usually employ excellent phase noise properties but the tuning range is restricted (i.e. max. +/- 50ppm). When larger tuning ranges are required the resonating element should be changed to another type of resonator like a high Q strip-line or coaxial ceramic resonator.

To extent the frequency range of the crystal based VCXO's the use of frequency multipliers is recommended. From approx. 800MHz onwards a VCO implementation by using coaxial ceramic resonator is possible.

3.2 Expected performance

Local Oscillator (LO) performance can be characterized in:

A) Long-term frequency stability

B) Spectral purity

C) Spurious Emissions

D) Output load characteristics

The expected (based on simulations/calculations) performance for each category will be discussed in the sections below.

3.2.1 Long-term frequency stability

With this the frequency behavior over temperature and time (aging) are meant. Since the LO generators output frequency is locked to the reference by a fixed ratio (N) the frequency drift performance is fully dictated by the reference signal assuming the LO generator is used within it's specified frequency and temperature range.

3.2.2 Spectral purity

Spectral purity, defined here as phase noise/ phase jitter. Phase Jitter being the integrated PN over given frequency interval.
The natural phase noise properties of the VCO inside the LO generator can be significantly improved inside used PLL bandwidth in case all noise sources in the system including the reference frequency phase noise are significantly below the synthesizers noise floor.

To calculate what will be the synthesizer noise floor we can use the formula from Philips technical paper [1] (13.05GHz PLL based LO generator in SiGe:C):

$$L(f) = FOM\left[dBc/Hz^2\right] + 20\log_{10} N + 10\log_{10} f_{ref} \quad \left[dBc/Hz\right]$$

When all other noise powers from sources inside the PLL, such as the PFD / freq. divider / charge pump and reference noise, are significantly below this synthesizer noise floor the PN levels inside the PLL bandwidth will be equal to L(f).

In the table below we can see the L(f) for VSAT LO=13.050GHz at the usable divider ratios.

N	L(f)	FOM	20logN	10logFref
16	-107.8	-221	24.0824	89.1149
32	-104.8	-221	30.1030	86.1046
64	-101.8	-221	36.1236	83.0943
128	-98.8	-221	42.1442	80.0840
256	-95.8	-221	48.1648	77.0737

Table 3.2.2.1, synthesizer noise floor for various divider ratio.

As we can see the noise floor decreases when the divider ratio is decreased (requires increasing reference frequency). This is under the assumption that the noise contribution from the possible noise sources, apart from the PFD noise, remain insignificant.

For the reference frequencies required for each divider ratio we calculate:

N	Fref [MHz]
16	815.6250
32	407.8125
64	203.9063
128	101.9531
256	50.9766

Table 3.2.2.2, required reference frequency for various divider ratio.

3.2.3 Calculation example for required reference phase noise

For VSAT the requirement is to have a BUC LO with maximum phase noise of –95dBc/Hz at 100kHz offset (over temperature and supply variations). This can be met if: 1) the synthesizer Noise Floor is sufficiently low and 2) the PLL loop bandwidth in that case is significantly larger then 100kHz.
According table 3.2.2.1 the noise floor of –95dBc/Hz can just be met at N=256, but in that case all other noise sources in the PLL should be sufficiently low in order not to degrade the PN at 100kHz. It also leaves no margin for temperature, production spread and other variations.
For this we recommend to use N=64, which creates sufficient margin. The reference frequency for the LO generator is then 203.90625MHz, what should be the required phase noise for this reference?

We can derive the required reference phase noise from the synthesizer noise floor and the divider ratio. Assuming the reference PN will be degraded by 20 times log (N) when up-converted to the final LO freq in the PLL, then to get the same level as the synthesizer noise floor we need –101.8dBc/Hz - 20 log (64) = -137.9dBc/Hz. When the reference phase noise at 100kHz offset is –138.0dBc/Hz the PLL will have a noise power from the reference of –101.8dBc/Hz, and a noise floor of –101.8dBc/Hz by the PLL. The two noise powers can be added as this is none correlated noise, resulting in a –98.8dBc/Hz noise power at 100kHz (assuming PLL BW >>100kHz). The synthesizer noise floor and the reference PN in this example will dominate the overall PN. In case we want the best possible noise performance the reference noise should be lowered by an additional 15dB (-152.9dBc/Hz @ 100kHz), then the LO PN will be –101.6dBc/Hz @ 100kHz offset.

A spreadsheet program to calculate the noise levels, the required ref. PN and resulting overall PN is available upon request.

3.2.4 Calculation example for required CUP loop bandwidth

The CUP loop filter has to be dimensioned such that:

1) it suppresses the pulses from the PFD to eliminate reference breakthrough;
2) it generates a stable loop;
3) it is fast enough to fulfill the “dynamic requirements”;
4) the CUP does not degrade the VCXO PN.

The loop bandwidth in a PLL system should be significantly smaller then the comparison frequency to allow sufficient reference breakthrough suppression assuming a simple 2nd or 3rd order filter has to be used.

There are no requirements on lock time found for VSAT BUC. This will allow any time constant in the loop.

Concerning the PN we have to know the properties of the dominating noise sources in the system. The free running VCXO PN and the PN properties of the reference clock are assumed to be dominating.

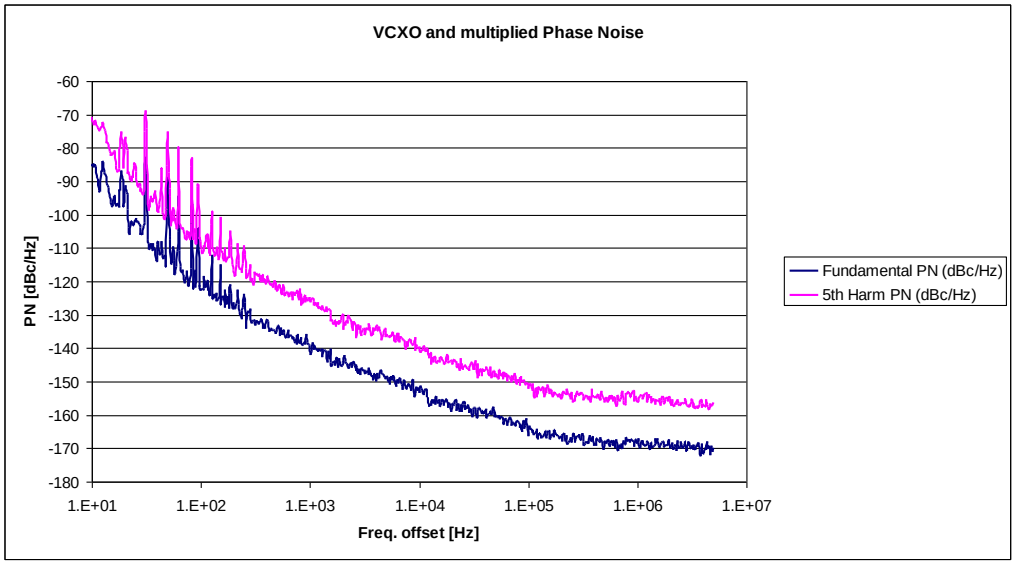

Fig 4. VCXO fundamental and 5th harmonic phase noise (free running)

Please note the low frequency spurious are coming from used PSU, using VCXO regulator will suppress them.

After multiplying the VCXO frequency by five we can expect at least 20*log(5)=13.97dB degradation in PN. From the results above this is confirmed.

If we calculate the PN values for the divided Fvcxo and divided Fref and the PFD noise floor it is possible to make an assumption for the final achievable PN.

In the table below we can see the phase noise at the CUP PFD, using the reference clock PN of <-125dBc/Hz at 100Hz (assumed), <-135dBc/Hz at 1kHz, <-140dBc/Hz at 10kHz (given by customer feedback).

Table 1. Phase Noise of VCXO and Reference clock calculated back to PFD
*by using formula PN = PN-20 * log(N), N for VCXO=1305, N for Fref. =64*

	External 10MHz ref PN	VCXO natural PN
100Hz	Max. –161dBc/Hz	Typ. –171dBc/Hz
1kHz	Max. –171dBc/Hz	Typ. –188dBc/Hz
10kHz	Max. -176dBc/Hz	Typ. -201dBc/Hz

As the (10MHz) reference clock worse case PN is approx. 10dB higher compared to the VCXO PN a loop-filter BW <<100Hz must be used such that the 10MHz PN will not dominate the final PN performance. With the loop-filter BW<<100Hz we may assume sufficient suppression at the comparison frequency (156.25kHz), probably ref. spur's will be dominated by crosstalk on supply lines and/or by parasitic electro/magnetical coupling.

3.2.5 Spurious Emissions

It can be expected that besides the required reference frequency also mixing products may appear at the CUP output, for example in case the reference is obtained by frequency multiplication. As there is no clock signal required for the CPLD we may expect spurious at the PFD frequency and the VCXO frequency in case a multiplier is used. In case a DC-DC converter is used in the power supply of the CUP application special pre-caution should be taken to suppress used switching frequency.

3.2.6 Dynamic response

What is the CUP response on steps i.e. in input frequency or supply voltage? What is the systems settling time? These items can hardly be found in the standards. As most applied systems are quasi stationary one can imagine once the LO is on frequency it remains such for the entire TX/RX on-time.

3.3 Demonstrator schematics

The demonstrator consists of a main board and a click-on VC(X)O board. The schematic of the main board can be found in section 8.2.

3.3.1 The PLD part

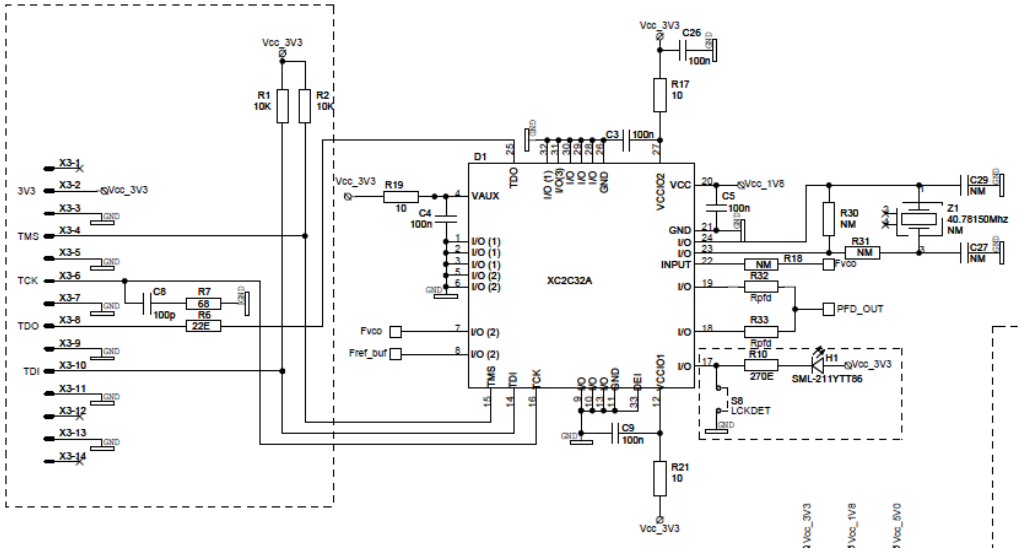

Fig 5. Schematic for PLD part

Used PLD can be programmed by JTAG connector X3, which is only required for the evaluation/development platform. For mass production there are possibilities to avoid this connector, please contact Xilinx for the details.
Two logical inputs are assigned, pin 7 and 8, one for the Fref (usually 10MHz) and one for the Fvco. For cost optimization the maximum input frequency to the PLD is limited (depends on the configuration/SW) and if required additional divide by two stages may be used.

3.3.2 Reference clock amplifier/converter

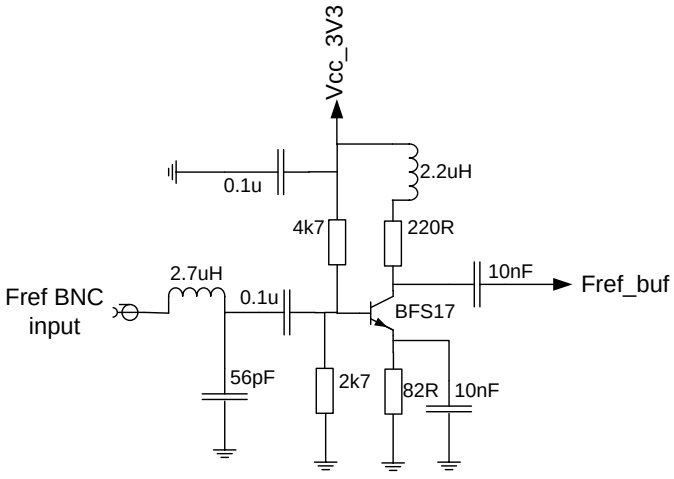

Fig 6. Schematic for reference clock amplifier / converter

This circuit amplifies the reference clock and generates a clipped sine wave from it such that the PLD can recognize the “zero crossings”. The BFS17 is biased at approx. 6mA, giving >25dB of gain at 10MHz! The 2.7uH inductor and 56pF capacitor create a <-10dB return-loss at 10MHz. See simulated gain/return-loss in figure below.

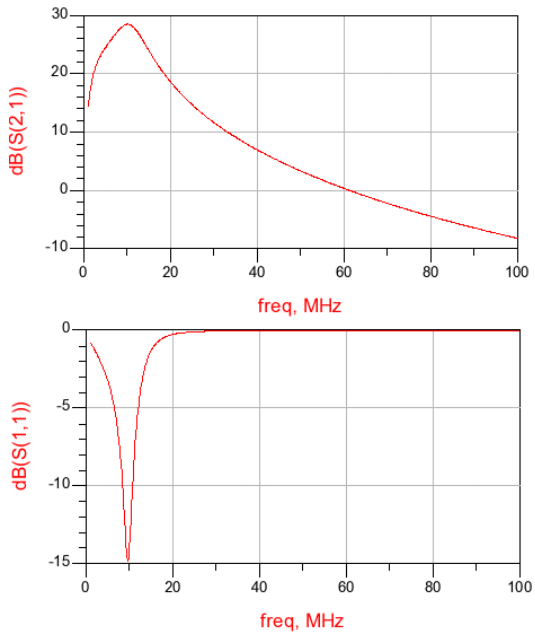

Fig 7. simulated S21 and S11 from reference clock amplifier

3.3.3 VC(X)O module / loop-filter

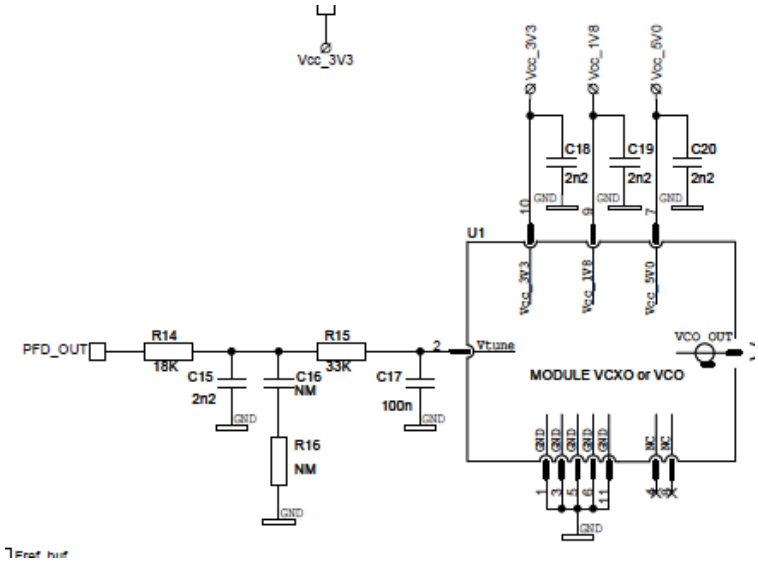

Fig 8. schematic for VCXO module / loop filter

Due to the modular approach the VC(X)O is a separate PCB that can be plugged on to the main CUP PCB. The VC(X)O module itself can be supplied by 1.8V, 3.3V or 5.0V to enable maximum flexibilty. The correction voltage, called Vtune here, comes from a circuitry that integrates the pulses coming from the PFD (implemented in the PLD).

3.3.4 203.90625MHz VCXO module

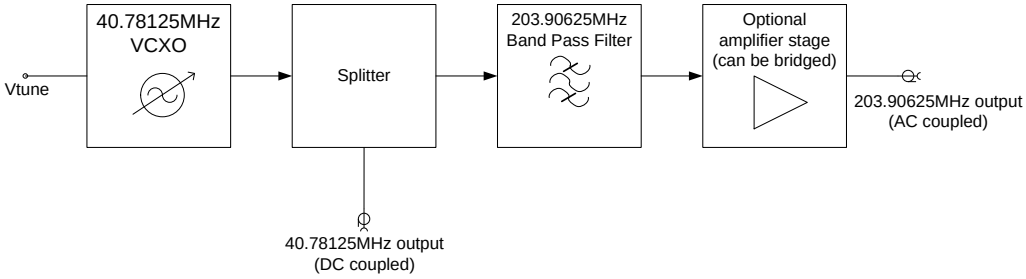

Fig 9. Block diagram for 203.90625MHz VCXO module

Crystals have superior Q factors hence potentially can meet the required PN when used as resonating element. Crystals with required characteristics to create a VCXO, at reasonable costs, are available from below 10MHz till approx. 60MHz.
As for VSAT BUC the recommended reference frequency is 203.90625MHz we decided to use a fundamental crystal at one-fifth of 203.90625MHz, which is 40.78125MHz. Positive side effect of this choice is that the fundamental frequency can be fed into the PLD (203.90625MHz would require a more expensive PLD part).
Please not that overtone crystal oscillators are very hard to tune in frequency, the $\delta F/\delta$loadcap is extremely small compared to the one for fundamental crystals.
A highly selective BPF filters out the 5th harmonic from the VCXO output signal. The VCXO output signal is basically a square wave containing strong odd harmonics.
The output of this BPF can be directly fed into the LO generator, or in case the output level is insufficient, be amplified on the VCXO module by an amplifier stage as described in section 3.3.4.3.

3.3.4.1 VCXO design

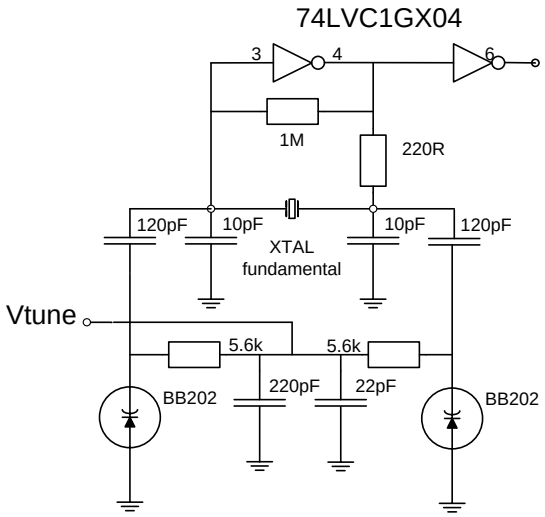

Fig 10. schematic for fundamental VCXO

The main block of the VCXO is a NXP 6 pin crystal oscillator/buffer 74LVC1GX04. Crystals for demonstrators are obtained from Tai-Saw Technology Co. Ltd Taiwan. The 1M resistor is to bias the inverters input at half Vcc, the 220R resistor limits the crystal drive power. The frequency of the oscillator is tunable by varying the load capacitance of the crystal. The total load capacitance is formed by the two varactors, the two 120pF capacitors, the two 10pF capacitors and some parasitic capacitance of the circuitry.

Please note that any noise/ripple on the XO supply might convert to excessive phase noise/jitter. For this reason it is very important to implement a clean noise and ripple free supply for this block. For example by using a separate regulator on the VCXO supply and using large capacitance, low ESR value capacitors.

3.3.4.2 Time domain properties

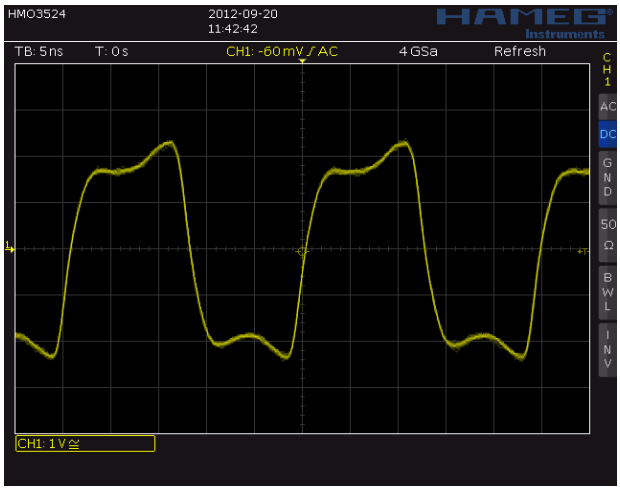

Fig 11. 40.78125MHz output signal in time domain measured by differential probe

Figure 11 shows the VCXO fundamental output signal in the time domain.

Ideally the VCXO block should have a rectangular wave shape output voltage that could be described mathematically as Vout = sin(ωt) + 1/3sin(3 ωt+φ1) + 1/5sin(5 ωt+ φ2) and so on. For the multiplier functionality we need to filter out the 5th harmonic only. In reality the wave-shape is not as ideal and contains odd and even harmonics depending on the symmetry in the time-domain of the signal. This symmetry depends on DC biasing and on the load impedance of the XO, not only at fundamental but also at the harmonics.

Please note that the output impedance of this XO block is not specified, it is expected to be relatively low impedance (voltage source by push-pull FETs). To avoid overloading the output special attention to the load impedance should be paid. The load impedance consists of the PLD input in parallel to the BPF input. The PLD input impedance is expected to be high Z, the BPF will be very reflective outside the pass-band (which is centered at the 5th harmonic).

3.3.4.3 Frequency domain properties

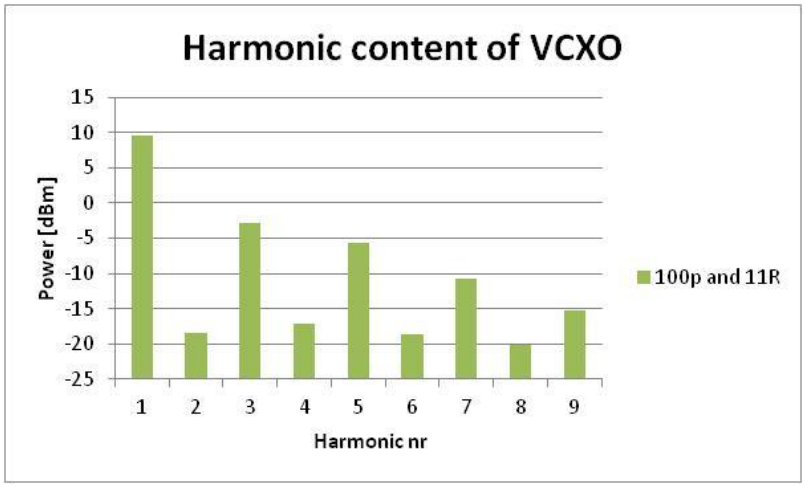

Fig 12. 40.78125MHz output signal in frequency domain (measured until H9)

Figure 12 shows the harmonic content measuring the signal by loading it with 50 Ohms (Spectrum Analyzer input impedance) and while the BPF remains connected (series capacitor 100pF). The power of H5 (fifth harmonic) is approx -6dBm. Please note that because of the loading with 50 Ohms the output voltage drops compared to the case when loading the VCXO by the PLD input.

3.3.4.4 Tuning properties

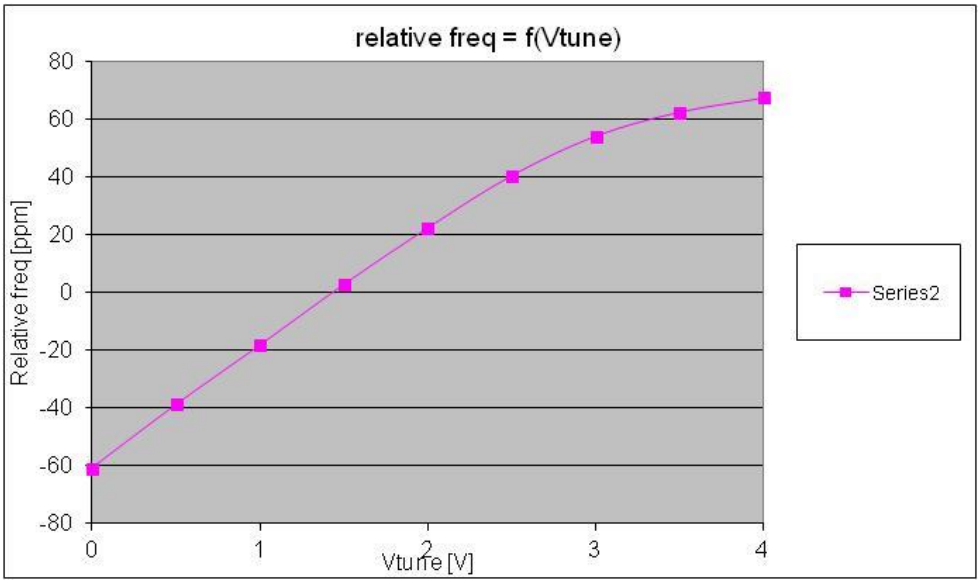

Fig 13. VCXO tuning characteristic

Figure 13 shows the relative frequency, referenced to 40.78125MHz, as function of the tuning voltage. For a well centered VCXO the nominal frequency is achieved at ambient temperature around 1.5V Vtune, leading to symmetrical margins.

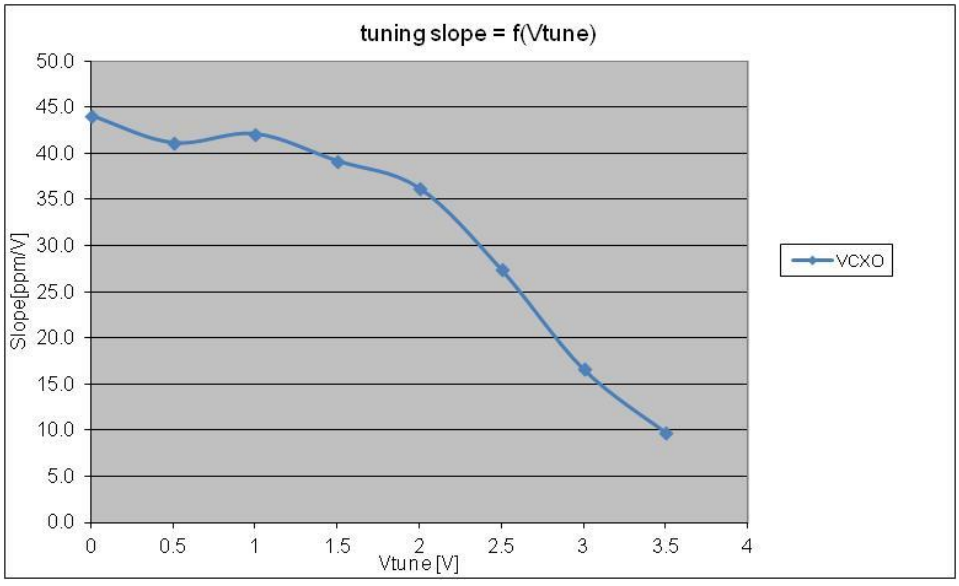

Fig 14. VCXO tuning characteristic

Figure 14 Shows the tuning slope, it is derived by differentiating the curve from previous figure. At the high Vtune side the slope degraded by a factor 3 to 4. When operated in this area the total CUP loop-gain will be lower hence the system response time and stability may be impacted.

3.3.4.5 Splitter / 203.90625MHz BPF design for 50 Ohms output system

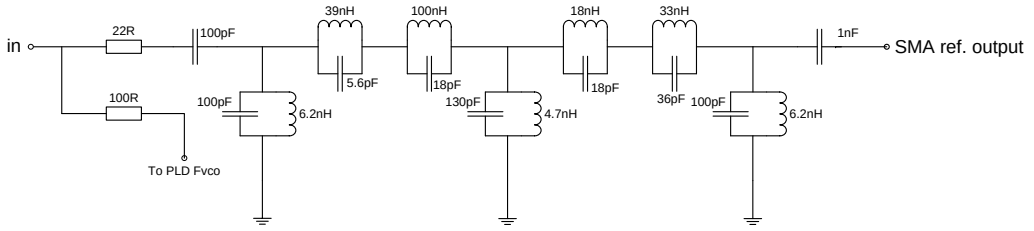

Fig 15. Schematic for splitter / BPF

The splitter consists of two resistors, one in the BPF=>TFF1003 (or equivalent LO generator) path, the other in the signal path to the PLD (or external divider in case required).
The BPF is a 7th order Cauer type, designed to avoid tight tolerance components or alignment. One can use various SW tools to simulate the response and calculate component values. For example Elsie, free student version available at www.tonnesoftware.com. It is important to suppress the fundamental VCXO frequency, as well as the (mainly odd) harmonics to avoid 40.78125MHz spaced spurious in the LO spectrum.

In the figure below the simulated S21 for the BPF is shown.

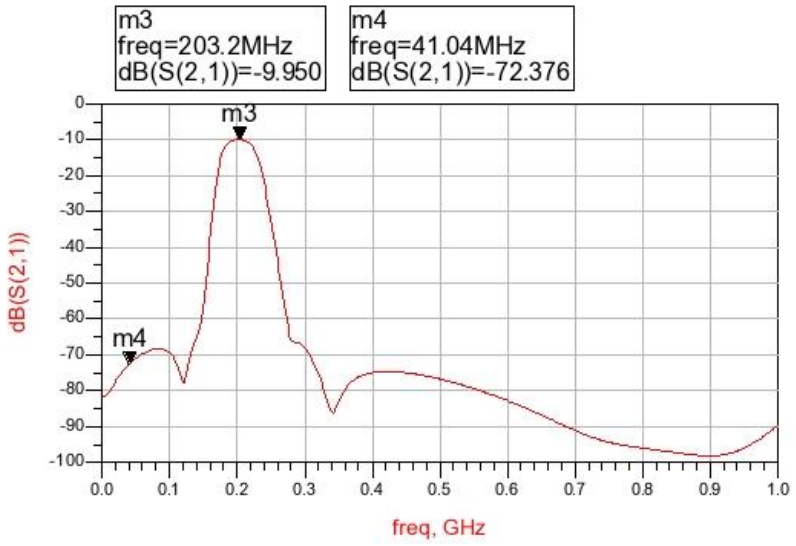

Fig 16. Simulated S21 for splitter / BPF (based on ideal inductors/capacitors)

It is important to perform simulations with the inductor models including parasitic. The SRF frequency and series resistance of the inductors might impact the performance. For phase noise measurement results on the free running VCXO/BPF see figure 4.

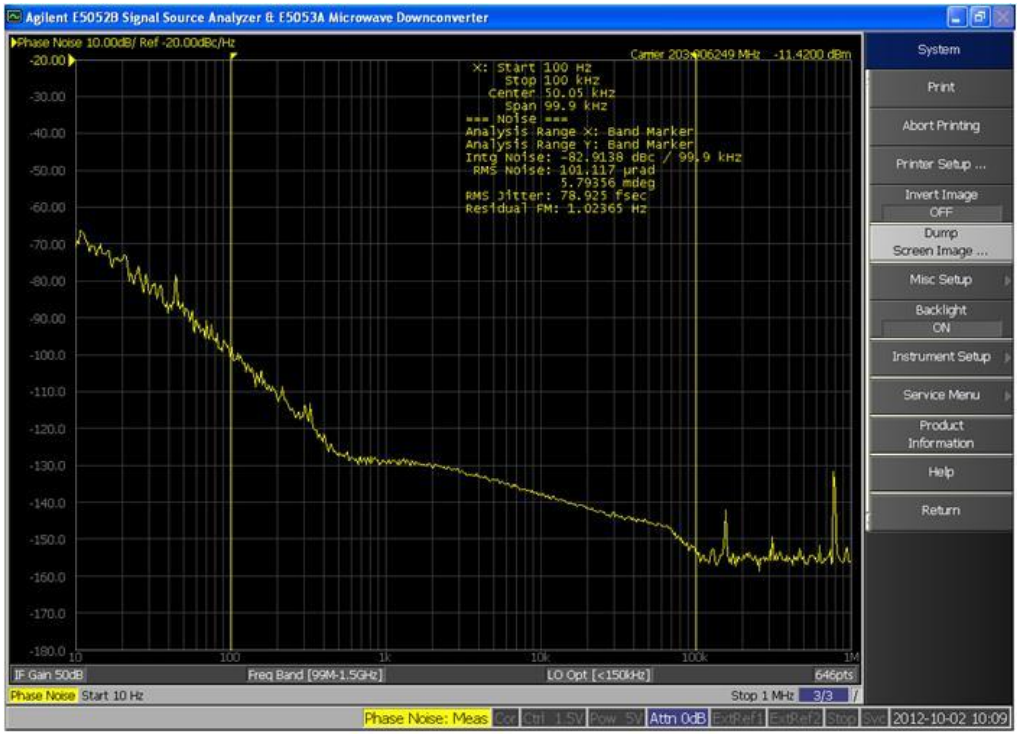

Fig 17. Phase Noise plot at 203.90625MHz when CUP is locking

3.3.4.6 Splitter / 203.90625MHz BPF design for high load-impedance system

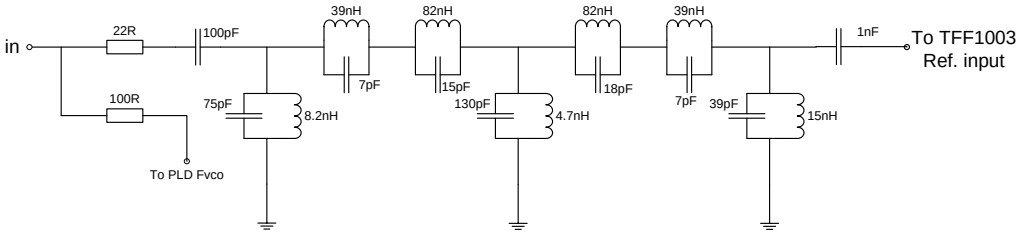

Fig 18. Schematic for splitter / BPF

The BPF can be modified in case the maximum output voltage has to be reached (to avoid the use of an external amplifier stage in the reference path. As the TFF1003 reference input impedance is several hundreds of Ohms the BPF can be adapted to get more output voltage out of it.

In case the transmission line from BPF output and TFF1003 reference input is short (electrical length <<0.2 applied wavelength) the BPF may be connected by a short PCB track. In that case the necessity for a transmission line with given characteristic impedance, i.e. 50 ohms, can be omitted. The 51 Ohms resistor to GND at the TFF1003 input should be deleted in that case.

The optimum input voltage for most NXP TFF LO generators is between 200mVpp and 600mVpp, with optimum implementation of VCXO and BPF approx. 300mVpp can be obtained.

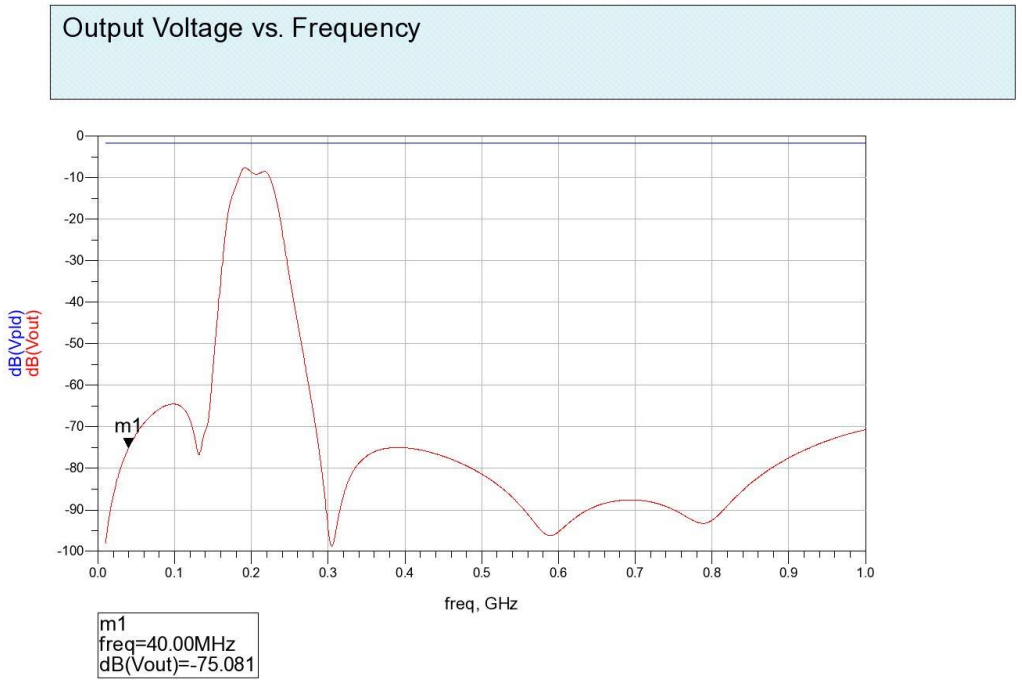

Fig 19. Simulation results for above shown BPF based on Murata 0603 components

For this simulation a rectangular source with 0R output impedance was used, fed into BPF with 22R series resistor and 100pF DC blocking capacitor. Load used was based on measured input impedance of TFF1003 paralleled with 150R.

3.3.4.7 Optional Fref amplifier design

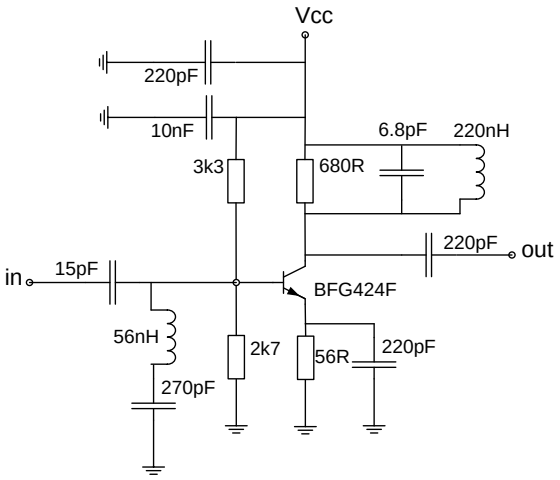

Fig 20. Schematic for Fref amplifier

Build around NXP BFG424F transistor, biased at approx. 8mA leading to >20dB of gain at 200MHz. Depending on the reference frequency, the losses in the BPF and the supply voltage of the VCXO this additional gain stage may be required. Please note that the drive level for the LO generator series is –10dBm < Pref < 0dBm (use attenuator in case Pout>0dBm). The figure below shows simulation results of the amplifier stage.

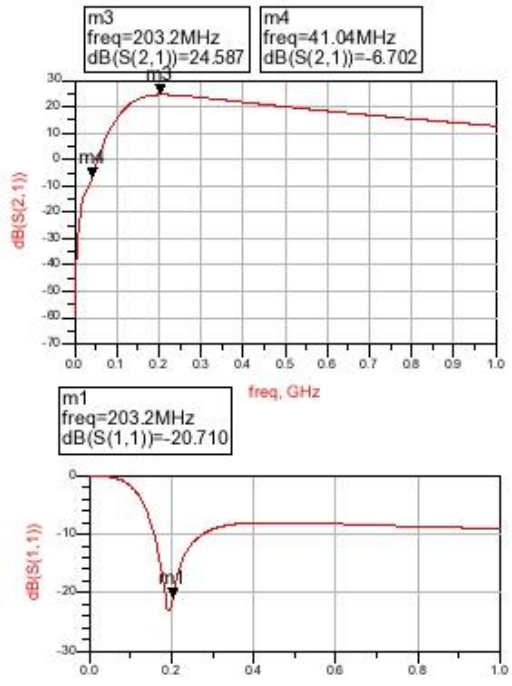

Fig 21. Simulated S21 / S11 for Fref amplifier

4. Practical information, setting up the demonstrator

4.1 Required measurement equipment

For measuring the key-performance parameters a minimum set of equipment can be:

1) A spectrum analyzer with sufficient low noise floor
2) A DC Power Supply Unit (PSU) with 3.3V output (200mA) and 5.0V output (100mA), preferably none switch-mode, low noise type
3) An signal generator for the 10MHz reference signal, output level 0dBm typical (-15dBm min.) In case the frequency and amplitude do not need to be variable the external reference from the spectrum analyzer can be used. Requirements on the PN for VSAT BUC: <-135dBc/Hz at 1kHz and <-140dBc/Hz at 10kHz offset.
4) An oscilloscope (preferably 100MHz or more)
5) A DCVM (multi-meter to measure voltages/currents)

4.2 Connecting / measuring the CUP

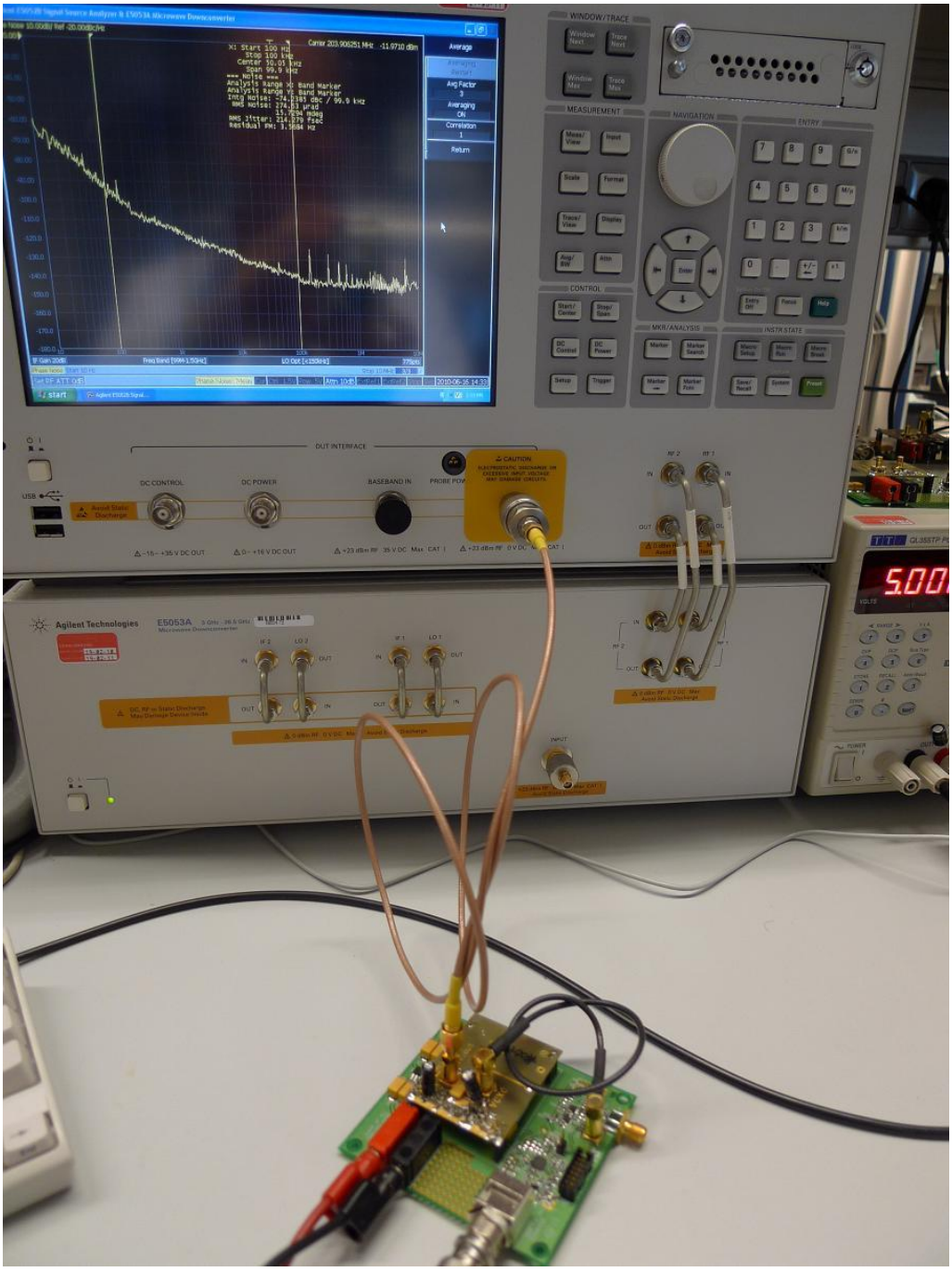

Fig 22. CUP demonstrator connected to phase noise analyzer

Connect the reference output to be examined to the input of the analyzer. Please note that the 203.90625MHz output of the VCXO board is AC coupled, but in case one wants to measure the 40.78125MHz output a DC block has to be used.

In case the nominal frequency has to be examined the 10MHz external reference output of equipment such as phase noise analyzer or spectrum analyzer can be used. For

measuring the lock range for example an external adjustable 10MHz source has to be used.

4.3 Connecting to the TFF100x/TFF11xxx demo-board

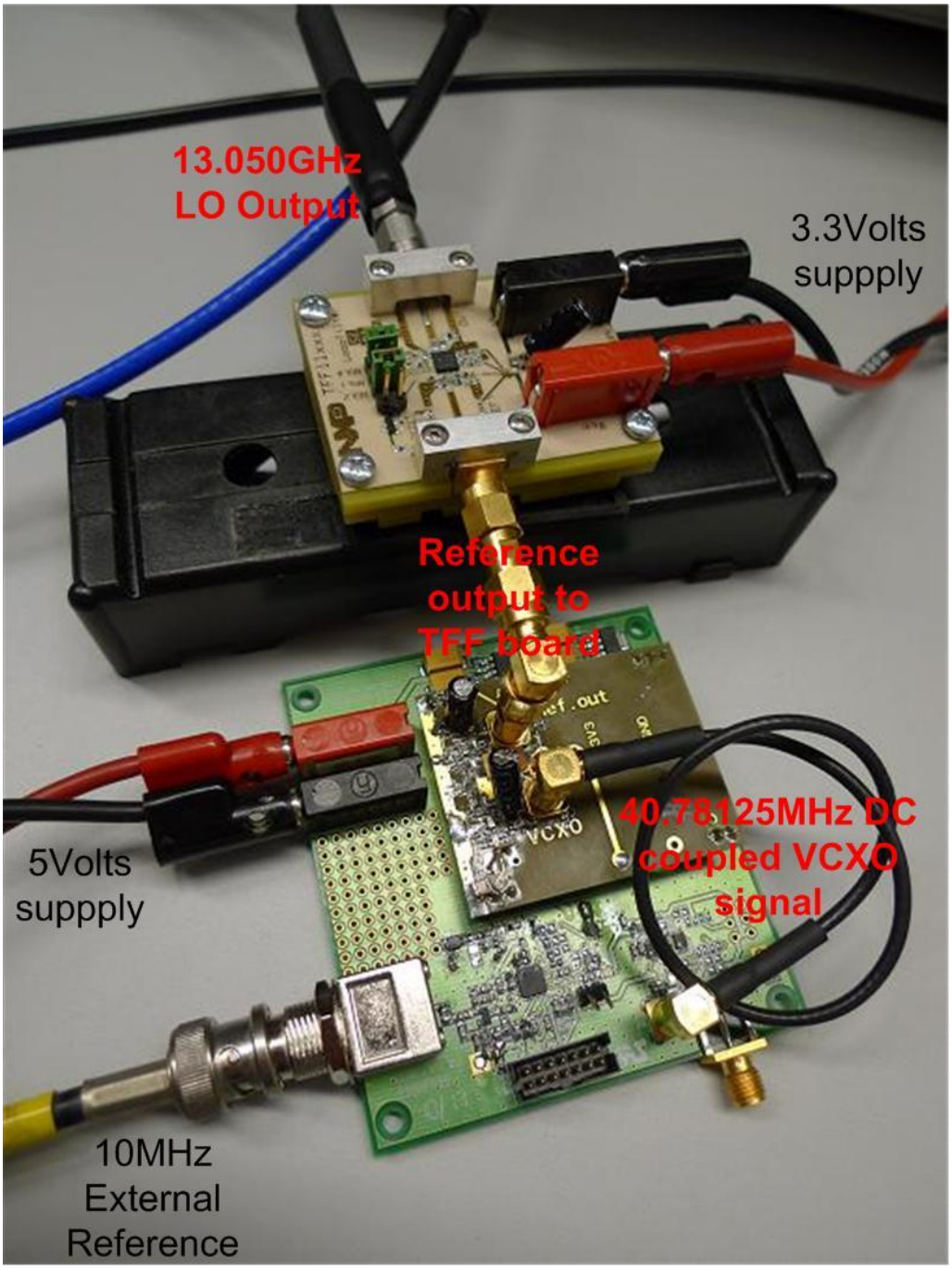

Fig 23. CUP demonstrator connected to TFF11xxx demoboard

Please note that the TFF11xxx/TF1xxxx demo-board and the CUP require two separate PSU units. It is important to keep the losses from the 203.90625MHz output of the VCXO board towards the TFF11xxx board as small as possible. Therefore an adapter piece was used (long cable would give additional losses).

When switch-mode PSU units are used excessive phase noise or spurious at the PSU switching frequency and it's harmonics might be observed. To check the PSU noise/ripple one can place a big electrolytic capacitor (i.e. 2200uF) on the supply leads close to the CUP banana sockets.

4.4 Connecting / measuring the system

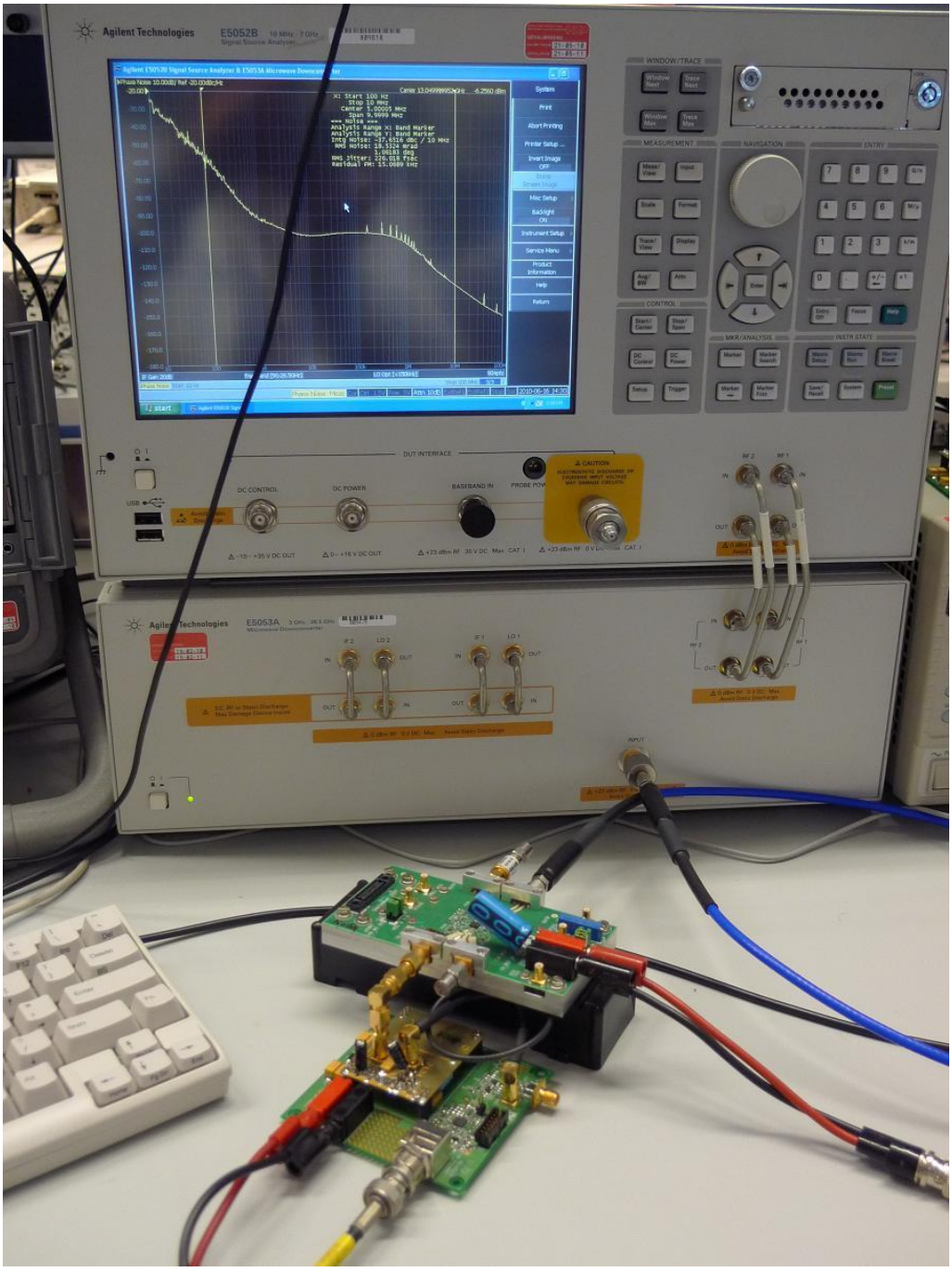

Fig 24. LO generator / CUP connected to phase noise analyzer

4.5 Frequently Asked Questions

Q: - the LO does not lock

A: - check the divider ratio set (three jumpers on TFF11xxx board)

- check the reference signal, power/lock
- check the tuning voltages for CUP and TFF11xxx, it should be between 0.2 and 2.9Volts for the CUP, 0.2 and 2.5V for the TFF1xxxx

Q: - the LO phase noise does not meet the required phase noise

A: - check the 10MHz reference phase noise in case close in PN is not met

- check with different PSU or additional large value decoupling capacitors on supply

5. PLD programming code

Software code to program the gates and latches inside the PLD to the right configuration is written in NXP PL RF small signal (VHDL code) with support from Xilinx Benelux. Various configurations that should lead to the same results are possible.

5.1 The Xilinx VHDL SW development environment

The ISE tool can be downloaded from the Xilinx web-site. For questions and support on the VHDL SW tool / code please contact Xilinx. The SW development environment looks like this:

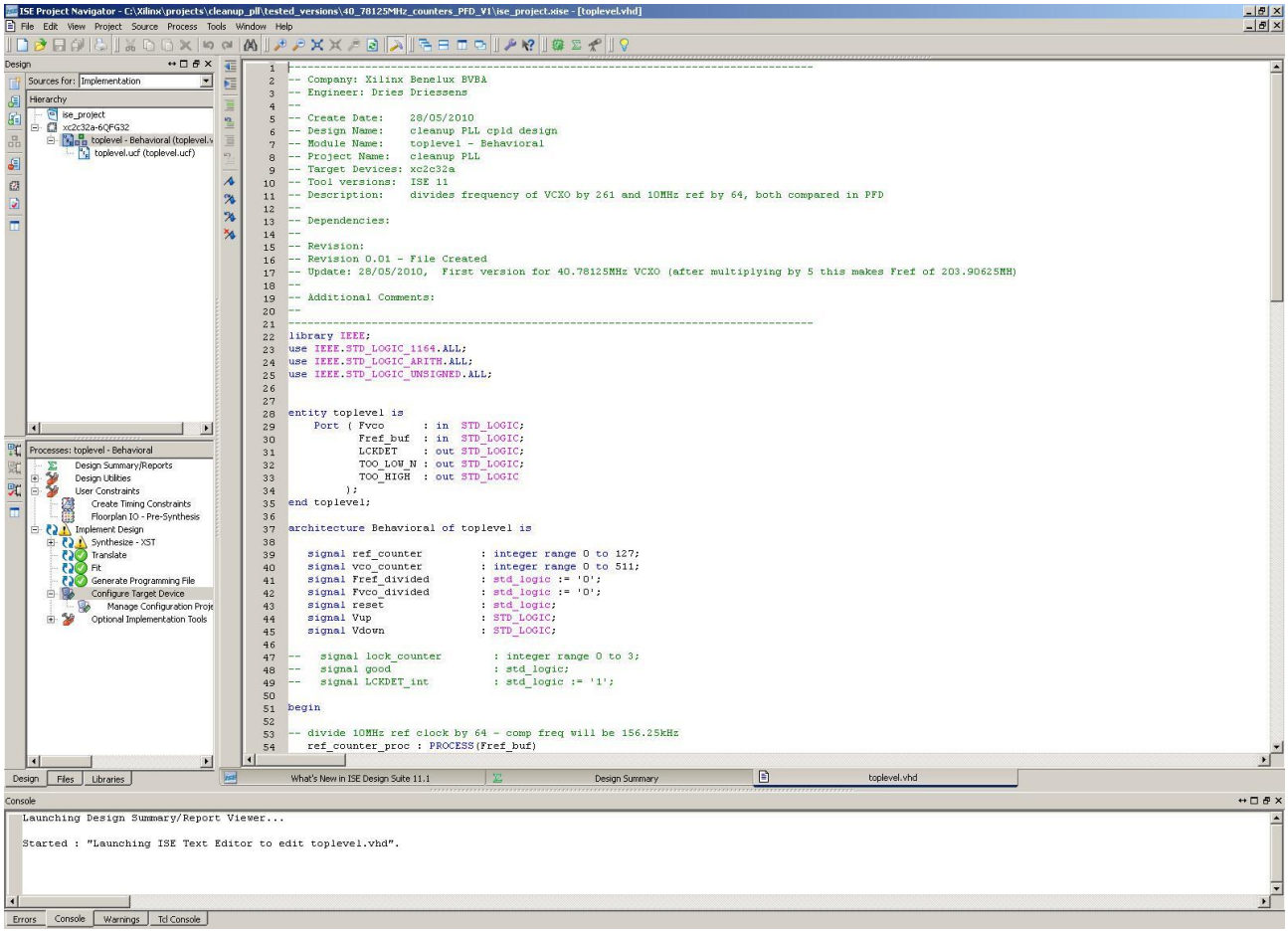

Fig 25. Xilinx ISE cockpit

5.2 Integer N implementation

The main code that is available is as described in the technical paper. In this configuration the incoming signal from the reference VCO(Fvco) is configured to a binary counter stage with N=1305, the external clock (Fref) is directed to a binary counter that counts in a loop of N=64. The output of both counters (a-symmetrical signal with frequency of 156.25kHz) is fed into the PFD.

Advantages of this integer N implementation is the simplicity (design time / processing speed), disadvantages are the probability of reference spurious and the limited possibilities in choosing the VCXO/reference frequency. Ultimately both incoming signals need to be divided down to 1Hz at which the PFD could work. This would limit the loop filter bandwidth to <<1Hz, which results in a very slow response time. The required amount of flip-flops would be impractical.

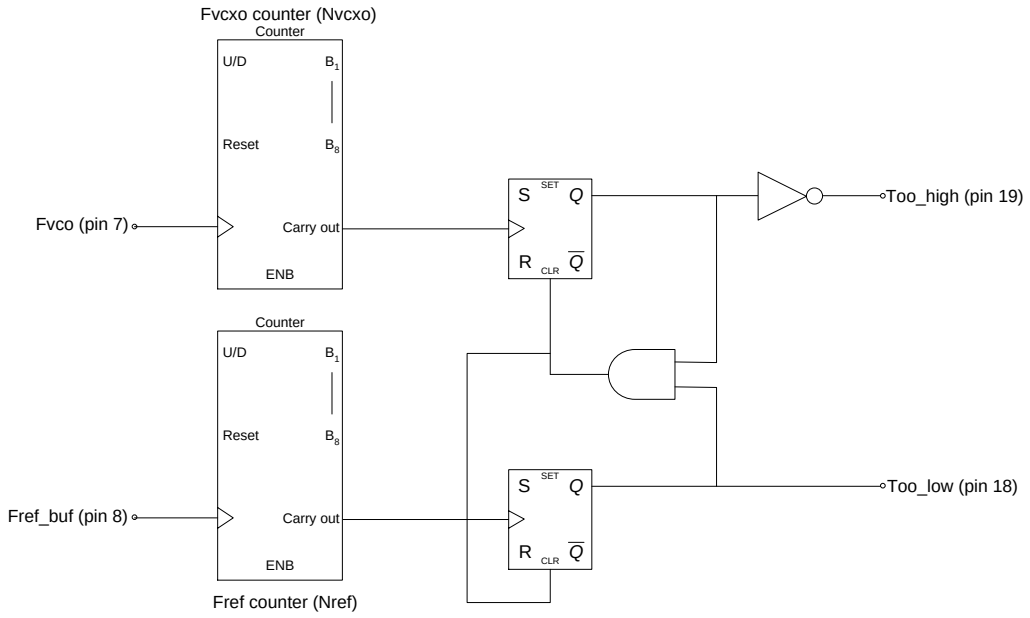

Fig 26. Hardware representation of integer N solution (VSAT: Nvcxo=261, Nref=64)

5.3 Fractional N implementation

To enable every possible output frequency and to increase the PFD frequency (could decrease the reference spurious) a fractional N SW implementation could be used.

If we want to run the PFD for example directly at the reference clock (10MHz) the main divider for the VCXO frequency has to be 40.78125/10=4.08725. There is an integer divider ratio of 4, the fractional part has to be 5/64. There are several techniques to implement a fractional N PLL that will not be discussed here. Theoretically the main divider is switched from one divider ratio to another in a certain sequence that spreads the spurious noise outside the LPF BW.

A SW code, based on sigma delta spreading, is available but due to the limited amount of gates inside the PLD the functionality/flexibility is restricted.

6. Measurement results

6.1 CUP reference phase noise at 203.90625MHz

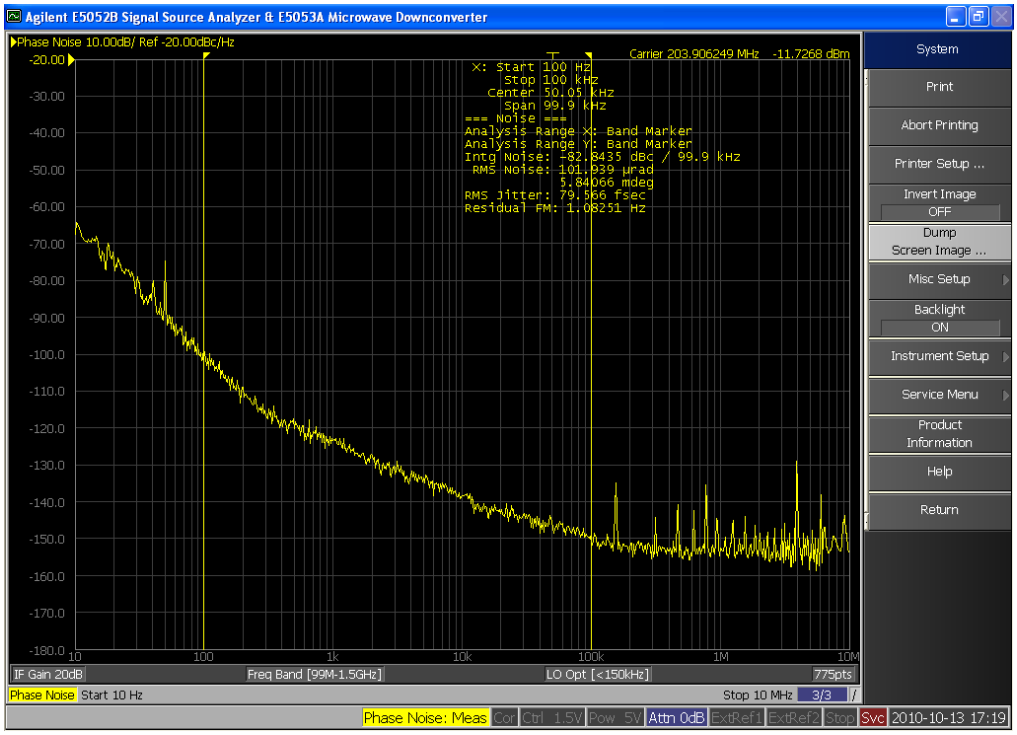

Fig 27. Phase Noise result at 203.90625MHz

As calculated in section 3.2.3 the synthesizer noise floor with N=64 and Flo=13.050GHz is –102dBc/Hz, when the reference PN is at 138dBc/Hz it will cause the same amount of noise power, resulting in –99dBc/Hz at 100kHz offset in the LO spectrum. As shown above the actual PN at 100kHz offset is approximately –150dBc/Hz, so the LO PN at 100kHz offset must be better then –100dBc/Hz as shown in the graph below measured at 13.05GHz.

6.2 System phase noise at 13.05GHz

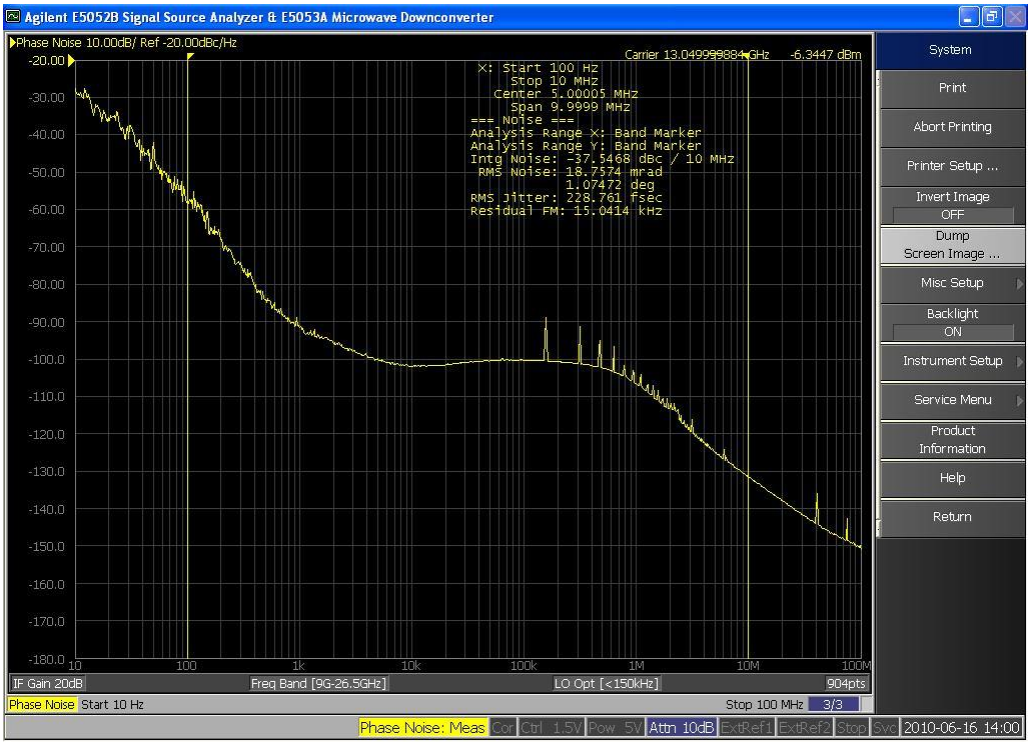

Fig 28. Phase Noise result at 13.050GHz

Please note that the integrated RMS PN (Jitter) at 13.05GHz is the jitter at the reference multiplied by used divider ratio in the TFF11xxx (15.5mdegr * 64 = 0.992 degr. RMS). The spurious observed in the graph are measured in a 1Hz BW, hence do not represent the proper “dBc value”. TO measure the relative spurious level (in dBc) a SA must be used.

6.3 Phase noise over temperature (at 13.05GHz)

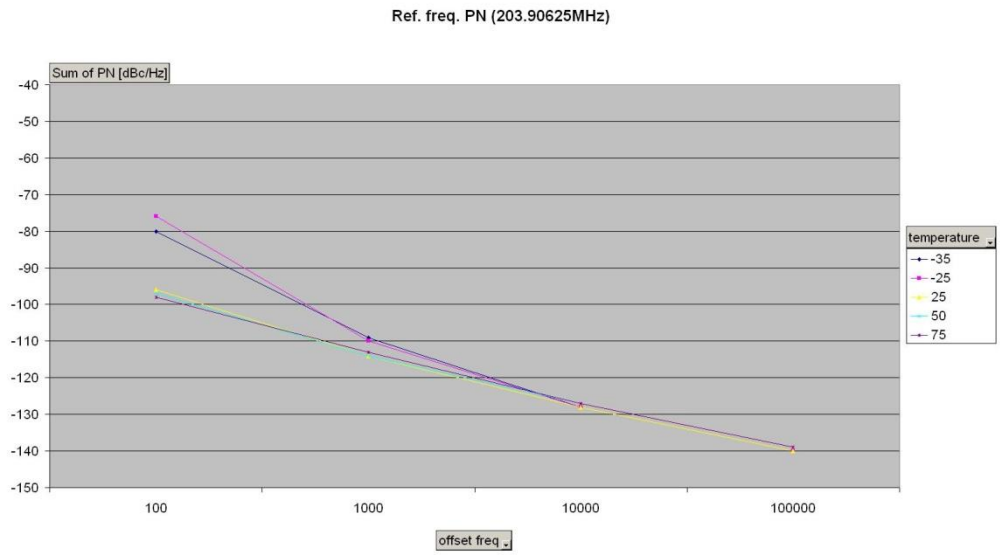

Fig 29. Phase Noise result at various temperatures (Flo=13.050GHz)

At extreme low temperatures some degradation at 100Hz offset is observed. This is very likely caused by the power supply decoupling, which is partly implemented by electrolytic capacitors. These kind of electrolytic capacitors may decrease significantly in value at extreme low temperatures. It is also important to choose “NP0 like” capacitors in the PLL loop filter or capacitors that do hardly change in value at extreme temperatures.

6.4 Locking range over temperature (at 13.05GHz)

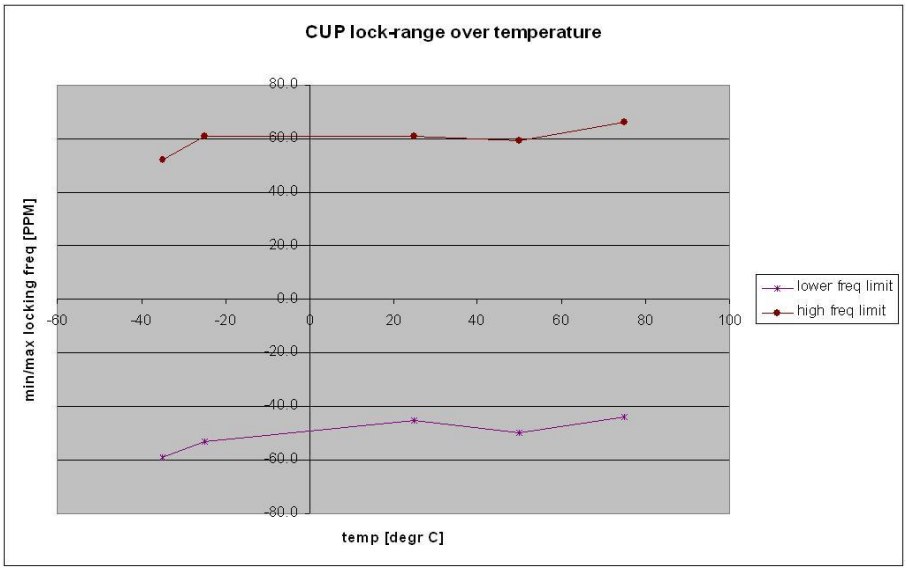

Fig 30. CUP lock-range over temperature

The required lock range of +/-25ppm (VSAT BUC) over the entire temperature range is met with sufficient margin.

7. Bill of Materials (BOM), supplier information

7.1 Semiconductors

7.1.1 Transistors, Varicaps and XO

NXP Semiconductors.

Table 2. NXP key-components used

Identifier	Type	12NC	amount	function
V1	BFS17	9330 827 71215	1	Amplifier 10MHz
VAR1, VAR2	BB202	9340 569 20115	2	Varicap VCXO
D2	74LVC1GX04GW, 125	9352 740 24125	1	Crystal oscillator
V2	BFG424F	9340 591 26115	1	Ref. signal amp (not always required)

7.1.2 PLD

Xilinx, partnumber: XLXXC2C32A-6QFG32C for 6nsec propagation delay device (Fref<150MHz), for increased freq. range also the 4nsec prop. Delay type can be used, **Part-number: XLXXC2C32A-4QFG32C**

http://www.xilinx.com/

7.2 Passives

7.2.1 Crystal

TSTS, Tai-Saw Technology Co. Ltd Taiwan

Part-number (for VSAT 40.87125MHz crystal): TZ1856A

TST Contact Person : Kevin Chang, oversea Sales Director
Tel : +886-3-4690038 ext 110
Mobile: +886-963019383 (TW)
+86-15814673863 (CN)

7.3 SMD inductors

For BPF: Murata LQW15A series

7.4 SMD capacitors

Murata or Yageo, mostly 0603, for VCXO mostly 0402

7.5 Software tools

Elsie for simulation of used BPF, http://www.tonnesoftware.com/ free student version.

Xilinx ISE for PLD related programming. See Xilinx website.

8. Appendixes

8.1 Reference frequency range for current NXP LO generators

				Divider Ratio N									
Product	min freq [GHz]	centre freq [GHz]	max freq [GHz]	256		128		64		32		16	
TFF1003	12.800	12.925	13.050	50.0000	50.9766	100.0000	101.9531	200.0000	203.9063	400.0000	407.8125	800.0000	815.6250
TFF1007	14.620	14.810	15.000	57.1094	58.5938	114.2188	117.1875	228.4375	234.3750	456.8750	468.7500	913.7500	937.5000
TFF1008	14.130	14.220	14.310	55.1953	55.8984	110.3906	111.7969	220.7813	223.5938	441.5625	447.1875	883.1250	894.3750
TFF11070	7.000	7.200	7.400	27.3438	28.9063	54.6875	57.8125	109.3750	115.6250	218.7500	231.2500	437.5000	462.5000
TFF11073	7.400	7.600	7.800	28.9063	30.4688	57.8125	60.9375	115.6250	121.8750	231.2500	243.7500	462.5000	487.5000
TFF11077	7.700	7.900	8.100	30.0781	31.6406	60.1563	63.2813	120.3125	126.5625	240.6250	253.1250	481.2500	506.2500
TFF11080	8.000	8.200	8.400	31.2500	32.8125	62.5000	65.6250	125.0000	131.2500	250.0000	262.5000	500.0000	525.0000
TFF11084	8.400	8.650	8.900	32.8125	34.7656	65.6250	69.5313	131.2500	139.0625	262.5000	278.1250	525.0000	556.2500
TFF11088	8.600	8.900	9.200	33.5938	35.9375	67.1875	71.8750	134.3750	143.7500	268.7500	287.5000	537.5000	575.0000
TFF11092	9.100	9.350	9.600	35.5469	37.5000	71.0938	75.0000	142.1875	150.0000	284.3750	300.0000	568.7500	600.0000
TFF11096	9.300	9.550	9.800	36.3281	38.2813	72.6563	76.5625	145.3125	153.1250	290.6250	306.2500	581.2500	612.5000
TFF11101	9.800	10.100	10.400	38.2813	40.6250	76.5625	81.2500	153.1250	162.5000	306.2500	325.0000	612.5000	650.0000
TFF11105	10.400	10.700	11.000	40.6250	42.9688	81.2500	85.9375	162.5000	171.8750	325.0000	343.7500	650.0000	687.5000
TFF11110	11.000	11.350	11.700	42.9688	45.7031	85.9375	91.4063	171.8750	182.8125	343.7500	365.6250	687.5000	731.2500
TFF11115	11.700	12.000	12.300	45.7031	48.0469	91.4063	96.0938	182.8125	192.1875	365.6250	384.3750	731.2500	768.7500
TFF11121	12.100	12.450	12.800	47.2656	50.0000	94.5313	100.0000	189.0625	200.0000	378.1250	400.0000	756.2500	800.0000
TFF11126	12.400	12.800	13.200	48.4375	51.5625	96.8750	103.1250	193.7500	206.2500	387.5000	412.5000	775.0000	825.0000
TFF11132	12.600	12.950	13.300	49.2188	51.9531	98.4375	103.9063	196.8750	207.8125	393.7500	415.6250	787.5000	831.2500
TFF11139	13.500	13.900	14.300	52.7344	55.8594	105.4688	111.7188	210.9375	223.4375	421.8750	446.8750	843.7500	893.7500
TFF11145	13.900	14.350	14.800	54.2969	57.8125	108.5938	115.6250	217.1875	231.2500	434.3750	462.5000	868.7500	925.0000
TFF11152	14.400	14.850	15.300	56.2500	59.7656	112.5000	119.5313	225.0000	239.0625	450.0000	478.1250	900.0000	956.2500
				min ref freq	max ref freq	min ref freq	max ref freq	min ref freq	max ref freq	min ref freq	max ref freq	min ref freq	max ref freq

Table 2, reference frequency range for current NXP LO generators

8.2 Main PCB schematic

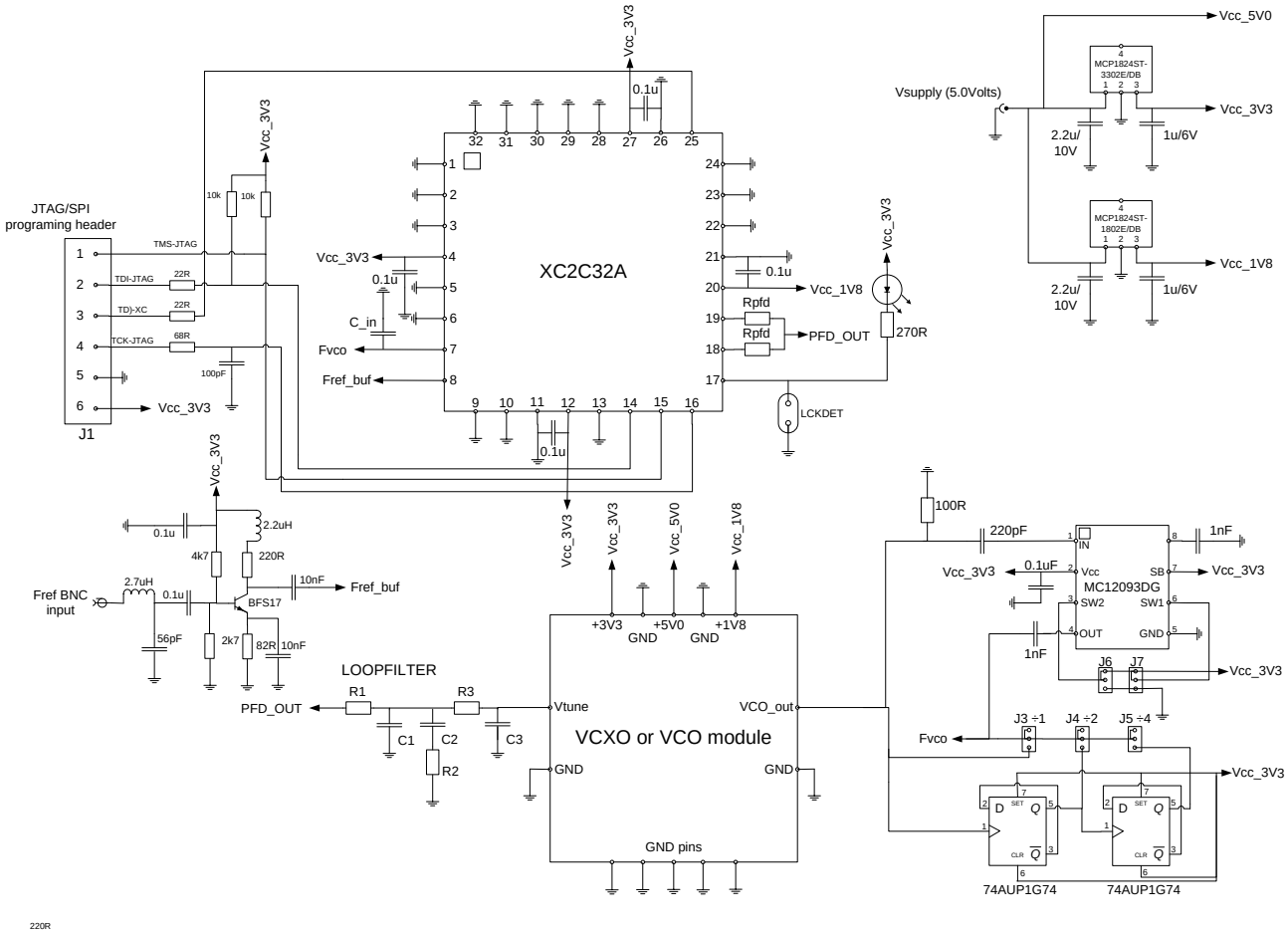

Fig 31. CUP motherboard schematic

8.3 References

[1]: technical paper NXP, “13.05GHz PLL based LO generator in SiGe:C”

8.4 Abbreviations

PN:	Phase Noise
CUP:	Clean-up PLL
VCXO:	Voltage Controlled Crystal Oscillator
SA:	Spectrum Analyzer
BPF:	Band Pass Filter

9. Legal information

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10. Contents

continued >>

UM TFF100x / TFF11xxx clean-up

generate CW reference for LO generators

For more information, please visit: http://www.nxp.com
For sales office addresses, email to: salesaddresses@nxp.com

Date of release: 04-10-2012

Document identifier: <DOC_ID>