White Paper

Freescale Technologies for Energy Efficiency

Energy Efficient Solutions by Freescale™

freescale semiconductor™

Overview

The design of an electronic system is almost always constrained by power and energy considerations—whether it is battery life for a mobile device, thermal power dissipation in a high-performance processor or ultra-low power consumption for a wireless sensing application. In addition, recent economic forces and increased environmental awareness have changed the landscape for new product design. Now, energy efficiency is often the lead discussion as companies formulate new product strategies. However, even though energy budgets are playing a larger role in determining the finished designs, manufacturers realize that the market will not allow them to compromise on performance. In response to these challenges, Freescale has adopted a comprehensive approach to optimize its products for high performance within constrained energy budgets.

This optimization is tackled across a broad front, including semiconductor process technologies, circuit design techniques, system architectures, platform configurations and design methodologies. For CMOS technologies, novel approaches are used to reduce both static (leakage) power and dynamic (switching) power. This is increasingly important as CMOS geometries continue to shrink and static power becomes an even larger portion of the total energy used.

As a result, Freescale is a recognized leader in the design of high-performance, energy-efficient semiconductor products. Underscoring this, Freescale has introduced the Energy-Efficient Solutions mark to highlight selected products that excel in effective implementation of energy efficiency technologies that deliver market-leading performance in the application spaces they are designed to address.

This white paper covers how Freescale technologies for energy efficiency are used to dramatically reduce power consumption without sacrificing performance and functionality, and highlights a selection of Freescale products that use these technologies to achieve exceptional overall energy efficiency.

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The Design Challenge

It's a balancing act. Manufacturers are trying to create products that push the limits of speed and functionality, yet they are expected to run on next to nothing. Tip the high-performance/low-power balance too far to one side and you will not satisfy the consumers who demand both performance and efficiency with few, if any, compromises.

One may think this balancing act applies only to portable devices—an MP3 player that runs all day but can download any tune in seconds and store thousands like it. But that's not true. Plugged or unplugged, applications designed today must consider the total cost of using energy and the impact any excess will have on the environment. For instance, in a 24-hour day, office appliances connected on a LAN will draw power continuously, but may actually "work" for only a few minutes, seconds or even microseconds. Therefore, it's just as important to optimize products for energy efficiency while they sleep as it is while they work. Consumers and businesses alike cannot afford to pay for any wasted energy.

Unfortunately, there is no single power reduction technique that is able to meet all the system requirements for energy minimization. The trick is to effectively combine architectural, platform and circuit techniques, system and application software, process technology and design methodology and tools to intelligently develop semiconductor designs for energy-efficient operation in all applications.

Freescale's Energy Efficiency Target illustrates how these technologies and techniques are integrated into the full development process designed to achieve optimal energy efficiency. Each area of technology can be optimized toward more efficient operation while still contributing to overall performance goals.

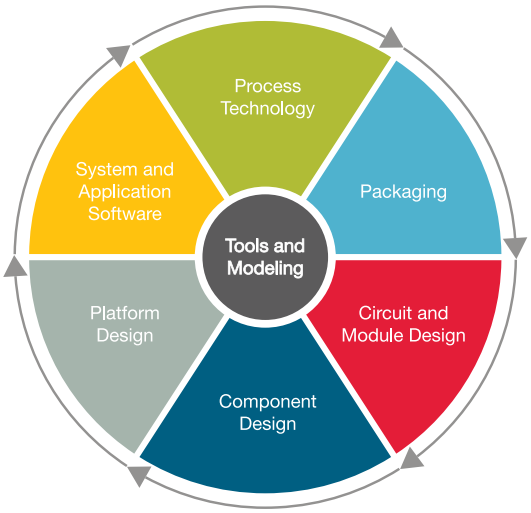

Figure 1. Freescale Energy Efficiency Target
The Freescale Energy Efficiency Target is a holistic approach to energy management, where interaction among the technologies and techniques is critical to achieve optimal energy savings.

As you investigate the following technology descriptions, keep in mind that they are all part of a unified development process that aims to maximize energy efficiency as an essential ingredient for any high-performance automotive, networking, industrial or consumer system.

Architectural and Platform Techniques

At the architectural level, energy efficiency technologies use circuit techniques to enable energy savings across the chip design. Using multiple power modes is a good example.

On-chip power modes are designed to offer peak application performance (and attendant energy consumption) only when absolutely necessary. To deliver optimal energy efficiency over the life of the application, on-chip power modes such as run, wait, stop and standby, are used to manipulate power usage to get the most efficient use of the available energy source. This is a particularly effective strategy for portable hand-held devices and office automation systems on a LAN that periodically engage in short bursts of activity.

Platforms are made up of a collection of component modules connected together for a specific purpose. A platform may be a collection of modules on a board, in a package or in a single semiconductor device. The combination of modules provides yet another opportunity for energy efficiency optimization.

For platform power modes, the power saving modes can be extended to board-level applications. For example, in a memory hold mode, everything can be powered-down except the PMIC and memory, which is kept in a state-retention mode. This is a very low-power state, and in many applications different components, such as an application or baseband processor, will have to reboot at wake up, creating some latency issues. However, if the core processor is kept in a low-leakage standby mode, wake up is much quicker because the baseband reboot won't be necessary. The application requirements will often dictate which memory hold state is used for best performance/energy efficiency optimization.

Circuit Techniques

To avoid forfeiting energy efficiency for greater application effectiveness we rely on an entire spectrum of circuit techniques, which when used in combination help regain the energy efficiency edge without sacrificing optimal performance characteristics.

- Dynamic voltage and frequency scaling (DVFS) allows on-the-fly frequency adjustment according to existing system performance requirements. By lowering the frequency, it is possible to lower the operating voltage (on-the-fly as well), dramatically reducing power consumption. There are two common implementations of this methodology—hardware-assisted and software-enabled. The DVFS hardware mechanism automatically monitors the processor load and controls supply voltage and frequency with minimal software and operating system involvement. Circuits without DVFS hardware can still implement DVFS through enabling software.
- Clock gating is an effective strategy that is widely used to help reduce power consumption while maintaining the same levels of performance and functionality. A circuit uses more power when it's being clocked than when the clock is gated or turned off. Clocks can consume as much as 40 percent of active power. By shutting off the clocks and stopping the data toggling in unused portions of the semiconductor we can realize sizable energy savings, particularly when the gating is engineered to control the toggling at the individual instruction level.

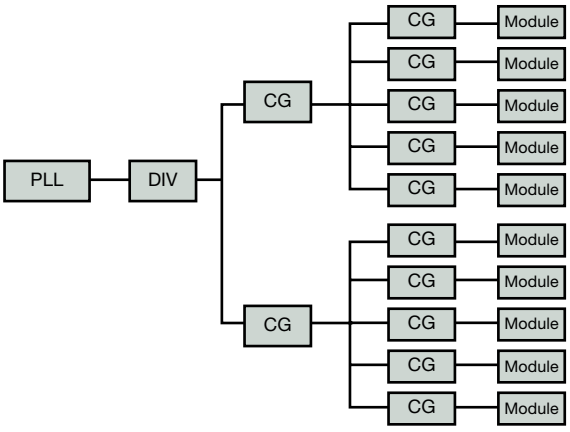

Figure 2. Clock gating
A typical clock tree where individual modules can be clock gated when not in use. Automatic clock gating control by the modules simplifies the software control.

- State-retention power gating (SRPG) is a technique that allows the voltage supply to be reduced to zero for the majority of a block's logic gates while maintaining the supply for the state elements of that block. SRPG can thereby greatly reduce power consumption when the application is in stop mode, yet it still accommodates fast wake up times. Reducing the supply to zero in stop mode allows both dynamic and static power to be removed. Retaining the supply on the state elements allows processing to continue quickly when exiting stop mode.

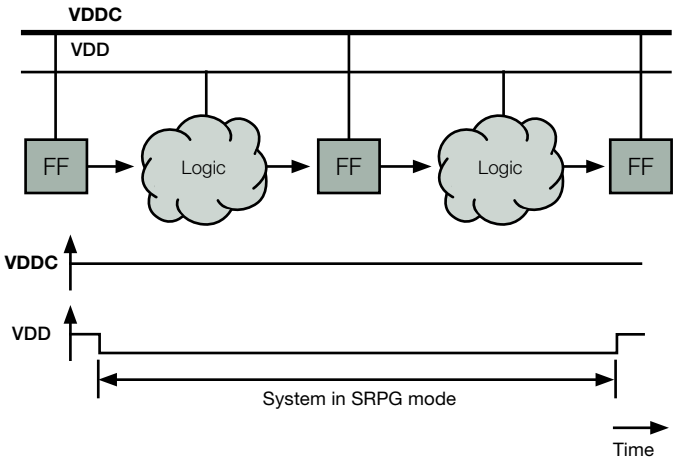

Figure 3: State retention power gating
Since the state of the digital logic is stored in the flip flops, if the flip flops are kept on a constantly powered voltage grid, the intermediate logic can be put onto a voltage grid that can be power gated. When the voltage is reapplied to the intermediate logic, the state of the flip flops will be re-propagated through the logic and the system can start where it left off.

- Our dynamic process temperature compensation (DPTC) mechanism measures the frequency of a reference circuit on the product. This reference circuit captures the product's speed dependency on the process technology and existing operating temperature. The DPTC then lowers the voltage to the minimum level needed to support the existing required operating frequency.

Regulator design is a special technique in which the design options are dictated by what's best for whatever application the solution is designed to serve. For instance, a switching regulator is more efficient than a linear or low-dropout (LDO) regulator. However, LDOs are not as costly (you don't need an inductor or other components) and inject less noise into the power supply line. They may be a better choice for radio frequency (RF) applications, where low noise is the dominant requirement.

Switching regulators normally operate at high frequency using pulse-width modulation (PWM) techniques. Under light load conditions, the switching regulator may transition to pulse frequency modulation (PFM) to maintain high power conversion efficiency. This technique, also called pulse skipping, allows high-efficiency switching regulation under light loads. PFM, with its longer cycle time, is slower to wake from a sleep mode. However, in applications where energy efficiency is critical, designers and users are normally willing to give up a little speed for a longer battery life.

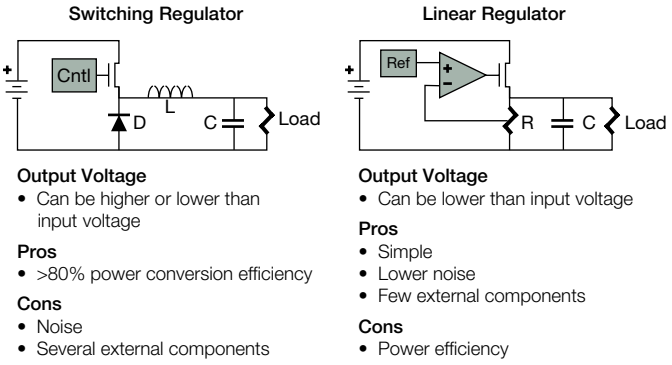

Figure 4: Switching and linear regulators
This illustrates the differences between switching and linear regulators.

Software

Software can play a significant role in how efficiently a system performs. Software-based power management provides a flexible and scalable framework that communicates with hardware through device drivers, manages use-case policies, models performance requirements real-time and responds to external interfaces and event notifications.

This framework allows the software to dynamically coordinate power-saving techniques across several hardware components. However, the efficiency of the software itself has a crucial impact on the power efficiency as well. Well-written code in addition to a well-optimized compiler will help reduce memory requirements and will lead to lower software overhead and reduced stack inefficiencies.

- Efficient code—Memory uses a lot of the system's power. Minimizing code can trim overall memory requirements and reduce power usage. Efficient code can also decrease OS overhead, such as entering and exiting tasks or servicing interrupts, and it can cut the number of wasted cycles, including pipeline stalls, cache misses and scheduling slack.
- Performance modeling—Heuristic and stochastic prediction modeling can be used to estimate the length of inactivity a device, subset of devices or an entire system will experience. Then, based on the implementation and policy in place, the model will decide whether to place the components into a low-power mode, reduce the operating clock frequency and system voltages or turn off the appropriate devices.

Performance modeling can also exploit the deterministic behavior of an RTOS to predict future power needs. Using the RTOS scheduling requirements, the system or various components can be placed in low-power modes or turned off if the expected idle time exceeds a specific time-period threshold. The software can also track active and ready-to-run functions and estimate how much processing power is required to meet any critical deadlines or minimum power levels.

- Dynamic power coordination—This process manages a database of registered devices and drivers, detailing their various power-related aspects, such as capabilities, states, associations (keyboard should prompt LCD to power on, etc.) and dependencies (device A should never be powered down when device B is in use, etc.). It also manages complex combinations of associations, dependencies, allowable power states and use cases based on a set of policy rules.
- In addition, dynamic power coordination can include priority-based task scheduling to ensure that time-sensitive work can meet deadlines while still maintaining low-power status. Tasks can be reordered or postponed, if non-critical, to allow more time-sensitive tasks to complete.
- Device management—The wonderful power-saving features built into the hardware are pointless unless they are effectively used. Software power management can communicate with the device drivers to:
  - Selectively control device power states and low-power modes
  - Enable DVFS
  - Provide functional clock gating and SRPG
- Event-based decisions—Software can respond to events (interrupts) instead of constantly polling for status. It can respond to a number of external inputs, including ambient light detection to reduce LCD brightness, various switches, closing lids (as in laptop PCs) and a variety of human-interface mechanisms.

Process Technology

Process technology is the basic building block of any semiconductor product. The characteristics of the process determine the power consumption of circuits built on that process. Our technologies for energy efficiency include process considerations targeted specifically for power-optimized circuit operations. Associated techniques for limiting power consumption include:

- Multi-VT process—Each transistor in a semiconductor design has an associated threshold voltage (VT) that determines the drive current of that transistor. A lower VT transistor offers higher performance because of the increased drive current available from that transistor. However, the electrical characteristics of lower VT transistors tend to make them higher leakage devices. Our manufacturing processes allow us to include both high and low VT transistors in the same chip. We can design our circuits using low VT transistors only for those critical paths that need the extra performance. The remainder can use higher VT transistors, which have the advantage of lower leakage current, which translates into lower standby current. In addition, Freescale uses innovative structures, materials and process techniques to optimize a transistor's performance while minimizing the leakage. These techniques are used to help improve the efficiency of all transistors, whether high VT or low VT.
- Active well bias—Well-biasing techniques help control channel leakage currents. Active well bias enhances the energy/performance relationship by manipulating transistor performance in real time. With an active back bias technique we use a low VT device for maximum performance, then raise the threshold in standby mode, thus providing two performance levels in one transistor.

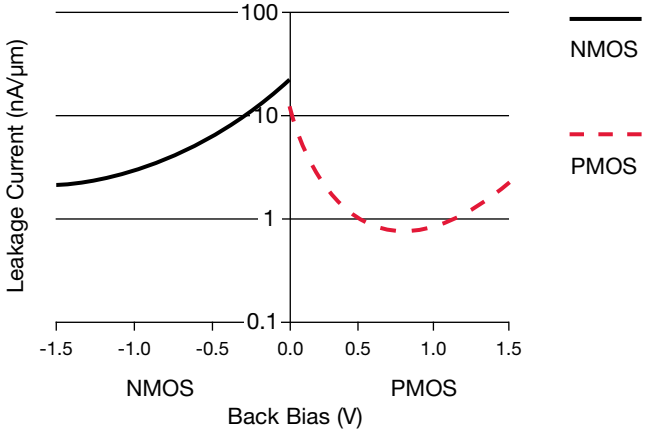

Figure 5: Active well bias
Active well bias affects the threshold voltage, which in turn affects the sub-threshold leakage currents. If the body of a PMOS device is increased above VDD or the body of an NMOS device is reduced below ground, the device is said to be in back bias and the sub-threshold leakage current can be reduced.

- SMARTMOS Technology—Freescale's hybrid processing and integration techniques offer another powerful tool to create highly energy-efficient devices. Our SMARTMOS technology enables high density analog/mixed-signal integration, highly efficient power MOSFETs and complex digital circuitry on a single die. It allows our power management IC (PMIC) solutions to incorporate load protection, high-power efficiency and multiple outputs—even as die sizes shrink—without eroding overall device performance. Introduced two decades ago, SMARTMOS technology has been scaled through multiple generations and is under continual development to improve its capabilities.

  Power MOSFETs must be conductive with low switching losses to achieve the most efficient use of the available power supply. Freescale's SMARTMOS technology allows for optimizing the MOSFET design for both drain-to-source resistance and gate charge control by making the gate oxide very thin along with using precise doping techniques to and achieve very low drain-to-source resistance.

The thinner gate oxide allows us to reduce the gate area on the silicon and minimize the charge required to drive the gate, thus reducing switching circuit losses.

Design Methodology and Tools

The physical mapping of the chip design can have a significant effect on energy efficiency by simply shortening the signal and clock routes. For instance, the global clock distribution design must appropriately manage the delays to the end tap points. A poorly designed, ad-hoc distribution may increase the amount of buffering necessary to correct skew at the tap points. This buffering can add to the power dissipation in the clock network. A well-structured distribution can lead to a more efficiently balanced clock tree.

Support/analysis, design, implementation, architecture and power estimation tools help ensure system-to-silicon IC design optimization across power, throughput, latency and area constraints. They help designers create a reliable methodology for energy-efficient semiconductor design, such as:

- Support/analysis—Library creation and characterization, along with power monitoring tools, helps support the module design and chip implementation teams as well as use-case power analysis.
- Design—Creating the modules used in the product design, tools assist in module functionality and power partitioning as well as module power estimation.
- Implementation—Integration optimization of all modules into a product. Tools include floor planning, synthesis, clock tree creation and embedded power, timing and power supply voltage (IR drop) analysis.

- Architecture—Performance/power trade-off analysis for inter- and intra-chip partitions plus use-case analysis.

A platform power estimation tool is used to combine the platform connectivity, the component architecture information, the module power data and the use-case definition into a common database to calculate the estimated power of the platform for a given application. The output of the platform power estimation tool breaks down the power usage per component and module to identify areas of the platform to optimize for overall power.

Energy-Efficient Technology at Work

High-efficiency embedded technology helps engineers develop automotive, networking, industrial and consumer applications that meet or exceed user expectations for low-power, low-cost operation. The benefits include longer operating times for portable applications, more efficient data centers and smart electric grids, which further enable plug-in hybrid electric vehicles, the seamless integration of renewable energy sources, adoption of green building standards and many other industry initiatives and applications.

Energy-Efficient Solutions by Freescale are specifically designed to lead the evolution of a more energy-efficient world by integrating the processes we've discussed in this paper to produce highly optimized platforms for the next generation of energy-efficient products and services.

MC9S08LL16 8-bit MCU

The S08LL16 is Freescale's most efficient 8-bit LCD controller, having less than 50 percent of the current draw of previous generation Freescale S08LC60 devices. Based on Freescale's QE family LVLP technology, the LL16 MCU demonstrates extreme low-power characteristics in power specs and power modes for battery-powered portable applications in the medical, consumer and industrial markets. The LL16 MCU achieves extraordinary low-power results through:

- An improved time-of-day (TOD) module with reduced functionality from previous modules (a simple quarter-second counter): less switching = less power. In addition, the peripheral logic runs at a reduced speed of 2 Hz rather than at the bus clock and the reset synchronizer is clock gated to reduce unnecessary power consumption.
- An improved internal clock source (ICS) with reduced-length clock traces between the ICS, oscillator and TOD modules: less length = less capacitance = less power.
- LVLP features shared with the QE family of MCUs include VLP oscillator, low-dropout standby regulator, 6 µs stop 3 wake up time, low-power run and wait modes, SATO, user-selectable peripheral clock gating and clock tree synthesis.

These low-power features enable consumer, industrial and wireless LCD applications that provide ultra-long life (up to ten years) using a variety of batteries, including AA, AAA, lithium coin size and 3.6V lithium. The LL16 has a rich LCD drive capability with internal RTC interruptions and other power-saving features:

- 1 kHz low-power oscillator used with a counter refreshes reference capacitor without being on all the time
- Low-power waveforms result in less frequent and less drastic transitions, which leads to lower power consumption
- Shoot-through current resistance circuit grounds switches before changing LCD bias levels
- Full non-overlapping clocks on LCD charge pump
- Optimized LCD driver circuit size for low-power LCD glass
- Distributed RAM at the LCD pins minimizes loading, which reduces the LCD driver's voltage domain
- Hardware display blink and alternating display modes without CPU wake

Based on the same testing environment, the LL16 LCD performance can provide over 70 percent improvement in power consumption compared to market solutions. For instance, with LCD segments configured ALL OFF with no contrast control, low-power mode, crystal oscillator enabled, 32 Hz frame rate, 4 x 22, the IDD is just 1.2 µA. With segments configured ALL ON with contrast control (3.08V) the IDD is still only 3.3 µA.

The S08LL16 MCU is an incredibly versatile LCD controller, not only offering low-power characteristics that broadens its target market to small, battery-powered applications but also providing improved design flexibility with a large segment-based 8 x 24 or 4 x 28 driver and an integrated charge pump to enable true system-on-chip functionality.

QE Family of MCUs

The QE family includes Freescale's lowest power MCUs and is the basis for other derivative low-voltage, low-power (LVLP) devices in the portfolio. The QE family of 8-bit S08 and 32-bit ColdFire V1 MCUs are particularly useful in consumer and industrial applications that require ultra-long battery life.

The LVLP process employs transistors with an increased channel length that reduces leakage current, which decreases static power consumption. We have subsequently optimized our standard cell library, which includes a number of low-power elements. LVLP features also include:

- Very-low-power (VLP) oscillator that consumes only 500 nA.
- Low-dropout standby regulator that enables low-power run.
- Low-power run and wait modes with regulator off.
- Wake up from sleep without reset.
- Stop 3 wake up time has been reduced from 110 µs to 6 µs, which means an application can wake up, perform a task and quickly go back to sleep to save additional power.
- Shared current reference and bandgap reduces the number of required transistors, therefore saving power and shrinking the silicon footprint.
- User-selectable peripheral clock gating enables energy-efficient optimization of the clock tree, which can consume up to 40 percent of the power used by the different modules.
- A self-timeout block (SATO), where flash memory is powered up long enough to perform a read with the result latched then automatically powered down. This process automatically kicks in at very low CPU rates and provides a much better (at low frequencies) IDD versus frequency curve for flash operation.

Freescale.com also features a battery consumption calculator for the QE family. Users can input different system parameters, such as device, environmental settings, battery information, duty cycle, system options and the number of active modules to calculate the average battery life for that system. It's a handy, easy-to-use tool that can help designers fine tune design proposals for maximum battery life.

The QE family of MCUs provides excellent solutions for portable battery-powered devices, such as digital cameras and camcorders, cordless phones, home health care devices and hand-held instruments. The family is also well-suited for low-power building automation applications, such as gas and water meters, thermostats, remote controls and security.

i.MX Family of Application Processors

The i.MX family includes ARM® core-based processors for automotive, consumer and industrial applications. i.MX processors employ Freescale's Smart Speed technology that uses hardware accelerators to offload the CPU and a 6 x 5 Smart Speed crossbar switch that nearly eliminates wait states. This enables fewer effective cycles per instruction, helping drive a performance equivalent to higher clock frequency processors without the power consumption penalty that accompanies higher operating frequencies.

i.MX application processor family members employ additional techniques to enhance energy efficiency:

- Clock gating, active well-biasing, DVFS, DPTC and SRPG.
- Multiple low-power modes, including wait, doze, state retention, sleep and hibernate.
- Clocking scheme designed to allow optimal frequency setting and clock source re-use for low-power applications.
- Space-division multiple access (SDMA) module and special busses connection allowing management of a number of data paths without OS involvement, keeping the CPU in standby mode.
- Integrated secure real-time clock (SRTC) allows shutting down the processor and power gating all supplies, except RTC supply voltage, while keeping the SRTC running and able to wake the system through a timer time-out event.

In addition, hardware accelerators are used for items that would ordinarily require heavy processing from the CPU, which saves power during run mode. i.MX application processors provide optimal power savings through integrated power management or paired with external Freescale power management IC solutions. Software development kits offer drivers for both the processor and companion PMIC to enable customers to successfully implement the low-power techniques in their final product designs.

MPC8536E PowerQUICC III Communication Processor

The MPC8536E processor is designed to implement office automation equipment (printing and imaging, network attach storage, media processing, digital signage and more) that require compliance to regional energy initiatives. These include such programs as Top Runner (Japan), Energy using Product (EU) and Energy Star (USA). In this capacity, the MPC8536E has accomplished a number of firsts:

- First Freescale PowerQUICC III processor that implements deep sleep mode in a single-chip SoC.
- First Freescale PowerQUICC III processor that implements core clock scaling (jog mode).
- First gigahertz SoC in the industry to provide a data path for network traffic during deep sleep mode with packet-lossless deep sleep.

The combination of fast run mode, jog mode and fast recovery from packet-lossless deep sleep mode creates a market-first embedded energy/workload pacing usage model. It's important to remember that the world is not just connected, it's always connected. This "net effect" is why carefully managing different performance cycles ("pacing" energy for long periods of inactivity interrupted by short burst of work) to fulfill application needs without losing the connection is so important. And this is what the MPC8536E processor is designed to do.

- Deep-sleep mode allows power to be removed from the Power Architecture® e500 core and L2 cache while the platform continues to operate. The enhanced three-speed Ethernet controller can continue to parse incoming packets, supporting lossless packet low-power operation with wake up on a user-defined packet, such as an ARP packet.
- Jog mode allows the core PLL ratio to be altered without rebooting the platform, supporting a low clock frequency for low workloads while dynamically switching to higher frequencies when the workload warrants.
- Doze, nap, sleep and deep sleep low-power modes with software-controlled device disable for explicit clock gating.
- A new long channel-length library was developed in addition to the multi-VT cell approach already used to enable gate-level power down, which greatly reduces static sub-threshold currents.
- Edge-rate control does not allow signals to transition slowly, improving short-circuit currents for all the receivers on the net.
- Block creation for minimal route length and efficient graph partitioning saves power by reducing the number of nets that are routed outside the blocks.

Traditional embedded computing platforms have been designed for maximum work load with little regard to the cyclical work profile across hourly, daily, weekly or extended time intervals. The MPC8536E is specifically designed to manage these cycles and pace the energy consumption for more economical automated office equipment.

MMA7660FC 3-axis Digital Output Accelerometer

The MMA7660FC accelerometer is designed to detect natural user interactions to enable advanced motion-based functionalities in hand-held devices, such as cell phones. These functions include such user-initiated actions as orientation, tap and multi-tap, shake and gesturing used to implement various commands as well as motion sensing for power-saving auto-wake and auto-sleep modes.

The MMA7660FC digital-output accelerometer offers extremely flexible performance/power consumption options through user-configurable sample rates. The rates can be adjusted to provide only the performance needed for specific functions, thus keeping current consumption to a minimum. For instance, at 120 samples per second the consumption rate is about 294 µA. However, if you drop down to one sample per second, the corresponding rate is just 47 µA. This flexibility allows developers to fine tune sample rates for specific functions, making sure the power consumption is as low as possible.

For example, 32 samples per second with a typical operating current of 133 µA is quite adequate to cover most shaking and gesturing requirements. However, 120 samples per second is advised for tap detection so the system can definitively recognize that it is a tap rather than a shake.

The MMA7660FC accelerometer also incorporates advanced automatic low-power modes with auto-wake (which can sample at 1, 2, 4, 8, 16, 32, 64 or 120 samples per second) and auto-sleep (1, 8, 16 or 32 samples for second). Toggling between wake and sleep modes is also configurable for even more power savings.

Three modes—off, standby and active—offer different capabilities for power-conservative applications.

- In off mode the digital line is on but the analog line is off. The sensor does not load the I^2C bus and all I^2C activities are ignored. Current consumption is 0.4 µA.
- In standby mode both digital and analog lines are on, and the sensor responds to I^2C activity. Registers can be accessed to set the device to active mode when desired, but the sensor measurement system is idle. Current consumption is 2 µA.
- In active mode both digital and analog lines are on, and the accelerometer responds to I^2C activity. The sensor measurement system runs at a programmable output data rate, and the digital analysis functions run. Depending on the sample rate, as discussed above, current consumption can be as low as 47 µA.

Sleep mode has a reduced sampling rate (tap mode is disabled) and I^2C activity will initiate auto wake to bring the MMA7660FC accelerometer to full active mode. The low-power modes and user-configurable sample rates make the MMA7660FC accelerometer an ideal solution for battery-operated applications, including hand-held portable communications, wireless sensors, game controllers and personal medical and sports monitoring devices.

MC56F8006/2 Digital Signal Controller

The devices in the MC56F8006/2 series combine, on a single chip, the processing power of a digital signal processor (DSP) and the functionality of a microcontroller unit (MCU) with a flexible set of peripherals to create an extremely cost-effective solution.

The MC56F8006/2 is the industry's first digital signal controller (DSC) demonstrating extreme energy efficiency for ultra-long battery life in portable applications using deep sleep modes, and provides the lowest power stop mode of any DSC in the market. It integrates a comprehensive, flexible set of peripherals to reduce the need for external components and create an extremely cost-effective control solution.

The MC56F8006/2 has been architected from the transistor level up to achieve low power consumption. Examples of this include:

- The DSP core employs a modified Harvard architecture with a multiply-accumulate (MAC) processor to achieve both single-cycle DSP performance and MCU capability, providing versatile control of end applications with high energy efficiency.

- It is manufactured with advanced process technology using Freescale's low-voltage low-power (LVLP) cell library, which is optimized for lower voltage operation and low device leakage to reduce static power consumption.
- An advanced power management module is implemented to support low supply voltage operation down to 1.8 volts (for certain applications) and to selectively disable circuit modules during stop modes. Standby current (Partial Power Down mode) is less than 1 uA and run current is less than 50 mA at 32 MHz.
- 56F8006/2 features a peripheral clock gating register that reduces power consumption by disabling clock signals to unused modules.
- The flash memory module switches to a low current mode at lower operating frequencies.
- Freescale's low-power design flow was used to implement and verify the system power-down methodology, and to predict and optimize power consumption to meet performance targets.

Specific energy and power management features of the MC56F8006/2 that enable it to meet a specified energy budget over the domain of the application include:

- Seven user-selectable power modes (run, low-power run, wait, low-power wait, stop, low-power stop and partial power down).
- Low-power wait and low-power run modes that can operate with all peripherals enabled.
- Dual 12-bit ADC optimized for fast, low-power data conversion.
- Clock options include an ultra-low-power crystal oscillator module, a 400 kHz relaxation oscillator, or a 32 kHz external oscillator. The 400 kHz or 32 kHz oscillators can be used with the post-scaler module to achieve ultra-low-power system operation at frequencies down to 125 Hertz.

MC56F8006/2 provides a cost-optimized solution for mathematically intensive, power-sensitive real-time control applications including power conversion, portable motor control, instrumentation, smart sensors and portable medical devices. The motor control and power conversion capabilities offered by these products can significantly improve the efficiency, reliability and energy savings of appliances and power supplies.

MPR031 and MPR032 Proximity Capacitive Touch Sensor Controllers

The MPR031/32 capacitive touch sensor controllers open up a new range of opportunities for touch control where it may not have been possible in the past. Generally, these kinds of applications are very small, often hand-held, require exceptionally long battery life and employ extremely simple electronic designs.

Such applications operate on very small energy budgets, which means the touch interface must also perform with minimal power consumption. The MPR031/32 capacitive touch sensors are state machine-based ASICs with inherently better power management than analog and microcontroller-based products.

- Unregulated internal power supply enables low-loss circuit operation.
- Precise low-power mode control for applications allows sample rates to be set, enabling the controller system to sleep during primary operation.
- Active low-power I^2C is functional for all low-power states. Thus, low-power implementation can remain active, even during communication cycles.
- 8 µA average supply current is the lowest in its class.

In addition, only one external component is needed, which not only reduces power consumption but also system-level material and manufacturing costs.

Conclusion

Ultimately, energy efficiency is measured against customer needs. Whether the application requires a longer battery life or needs to reduce heat dissipation, system designers have to rely on semiconductors that meet their performance requirements without exceeding a limited energy budget. We work very closely with our customers to clearly define the performance and energy parameters they require. Through close cooperation, we can optimize our solutions to help them make energy-efficient designs that are easy to develop, speed time to market and are more attractive to their customers.

Freescale technologies for energy efficiency are distinctive combinations of advanced architectural and circuit techniques with the latest design methodology and process technology that deliver energy-efficient performance. Freescale applies these technologies and techniques to provide the highest possible performance levels within a restricted energy budget. They can apply to any application, benefiting the user by extending battery life without significantly impacting performance in portable applications as well as keeping energy costs lower and heat dissipation down in wireline applications across all industries.

Freescale is dedicated to expanding our technologies for energy efficiency, developing new techniques for next-generation products that are even more energy efficient than today's. We are continuing to work with our customers and our business partners to help you produce more work using less energy.

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